Signal Integrity Enhancement in Digital Circuits
In the Presence of Power Grid Activity

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Abstract – As IC technology scales down, problems like power supply voltage transients may dramatically contribute to signal integrity loss. As a consequence, performance degradation, reliability problems and ultimately, functional errors may occur. In this paper, a new methodology to enhance SoC signal integrity with respect to power/ground voltage transients, without degrading its performance is proposed. The underlying idea is the dynamic adaptation of clock duty-cycle (CDC) to the variation of propagation delays along the disturbed logic paths. CDC modulation according to abnormal power grid activity is achieved by using positive and/or negative edge clock stretching logic (CSL) blocks. Using the proposed methodology, digital circuits become more robust to power line fluctuations while maintaining at-speed clock rate. Under severe V_{DD} variations, which ultimately require clock frequency reduction, CSL blocks avoid signal integrity loss when fast V_{DD} disturbances occur. Experimental results based on SPICE simulations for simple combinational, pipeline and FSM circuits are used to demonstrate the assertions.

Index Terms: signal integrity; power-supply transient; signal propagation delay; adaptive clock duty-cycle.

1. INTRODUCTION

Signal integrity is the ability of a signal to generate correct responses in a circuit. It generally includes all effects that cause a circuit malfunction due to the distortion of the signal waveform [1]. A good integrity signal presents: (i) voltage values at required levels and (ii) level transitions at required times. For instance, in a flip-flop with good signal integrity the setup and hold times are met.

Various signal integrity problems have been studied for high-speed gigahertz nanometer System-on-Chip (SoC). The most relevant are: (a) crosstalk (signal distortion due to cross coupling effects between signals) [2] (b) overshoot/undershoot (momentarily signal rising/decreasing above/below the power supply voltage (V_{DD}) and ground (V_{SS}) lines); (c) reflection (echoing back a portion of a signal, at high-frequency circuits, where interconnections behave as transmission lines); (d) electromagnetic interference – EMI (resulting from antenna properties) [3]; (e) power-supply noise [4]; and (f) signal skew [5][6].

This work focuses power supply disturbances, regardless of their origin, and their impact on digital circuit
performance. Both $V_{DD}$ depletion and ground elevation increase propagation delay in signal paths. Problem complexity increases when power management techniques that dynamically reduce $V_{DD}$ to minimize power consumption are considered [15]. These techniques are referred as Dynamic Voltage Scaling (DVS).

Many design solutions have been proposed to enhance signal integrity in the presence of power grid activity. Some of the proposed solutions include: 3-D layout modeling and parasitic extraction [8]; accurate RLC simulation of on-chip power grid [5] using decoupling capacitors [4][9] and to improve resistive voltage drop (IR-drop) [5][10]; insertion of buffers on the grid [8]; and shielding wires (e.g., grounding every other line) [11]. Buffer insertion and transistor resizing methods have been proposed also [12] to achieve better power-delay and area-delay trade-offs. Additionally, self-test methodologies and on-chip probes to monitor intra-packaging EM-emission activities [13] have been developed to test signal integrity in high-speed SoC. Finally, other techniques have been proposed, the reduction of the maximum distance between supply pins and circuit supply connections [14].

However, none of the above-mentioned techniques guarantees a perfect solution for the de-synchronization effect that result from the modified propagation delay in the presence of $V_{DD}$-$V_{SS}$ disturbances. A technique that addresses the problem of de-synchronization in memory elements (for pipeline based circuits) is proposed in [15]. In this case, the objective is to correct (not to prevent) errors caused by aggressive DVS techniques and to reduce power consumption.

Undesired $V_{DD}$-$V_{SS}$ transients in power grid may be constrained, but not eliminated. In order to guarantee correct timing performance in their presence, the ultimate solution is to reduce the clock signal frequency. However, for some applications, system performance degradation cannot be tolerated.

In this paper, a new solution, which does not require clock frequency reduction, is proposed. Its underlying principle is to dynamically adapt the clock duty-cycle (CDC) to the variations of propagation delay through the logical path whose power supply voltage is under disturbance. By doing so, it is possible to control, dynamically, the instant of occurrence of the clock edge that triggers the memory cells with the smallest time slack margin.

Another problem is that clock signal generators (like PLL) need time to reduce clock frequency, when a severe $V_{DD}$-$V_{SS}$ disturbance occurs and such reduction is mandatory for reliable operation. The proposed methodology increases circuit tolerance when the disturbances start to occur, allowing clock generators to react and reduce their frequency, without signal integrity loss.

This paper is organized as follows: Section 2 shows how stretching CDC can enhance circuit tolerance to $V_{DD}$-$V_{SS}$ disturbances. Section 3 describes the proposed methodology and introduces the basic concepts related to the CSL (Clock Stretching Logic) block. This section also presents the applicability situations and the basic principles for the application of the proposed method. In Section 4, experimental results are presented. Finally, Section 5 outlines the main conclusions of the work and directions for further research.

2. CLOCK DUTY CYCLE STRETCHING

A main advantage of the proposed methodology is to render the circuit more robust to power line fluctuations by insuring at-speed clock rate. As such fluctuations are often due to circuit operation, they tend to cause local disturbances in the power grid. Hence, it is a waste to reduce the clock frequency in the overall system; instead,
local solutions should be considered.

The proposed methodology uses a CDC modulation (CDCM) circuit that monitors the power supply voltage and adapts clock duty-cycle. The correspondent block is referred as the CSL block. CDC is locally adapted without losing circuit performance.

As pointed out, lowering the power supply voltage, \( V_{DD} \), enhances the propagation delay of related signal paths. Hence, lowering \( V_{DD} \) while maintaining nominal clock period, \( t_{CLK} \), reduces circuit noise and time margins, which will, ultimately, induce the occurrence of system functional errors. The time margin is characterized by the time slack, \( t_{PM} \). In this work, the time slack is defined as the difference between the clock period and the time response of the critical path in the slowest combinational module between registers.

A phenomenon of similar effects on the circuit timing behavior is the **ground bounce**, also known as **simultaneous switching noise**. This phenomenon occurs when internal nodes of a logic device change state. When this happens, the charge remaining in the internal nodes (\( C_L \)) is drained through the ground grid. The currents associated with this charge removal are added to the switching currents flowing from \( V_{DD} \) to the ground interconnects due to the simultaneous switching of the N- and P-networks. Thus, the resulting total current flowing through the ground grid induces a local voltage variation, namely, the ground bounce, \( V_{GB} \). Worst case conditions exist when a large number of nodes simultaneously switch. In this case, the resulting switching currents from each node capacitance are added together. The total current flowing through the ground lead reduces noise margins and increases the probability of system malfunction.

For the sake of simplicity, we normalize the size of the disturbance on \( V_{DD}/\text{ground} \) interconnects voltage using the parameter \( \gamma \) defined as follows:

\[
\gamma(\text{vdd}) = \frac{\Delta V_{DD}}{V_{DD_{nom}}} \quad \text{or} \quad \gamma(\text{gnd}) = \frac{\Delta V_{SS}}{V_{SS_{nom}}}
\]

where: \( \Delta V_{DD} \) is the difference between the nominal \( V_{DD} (V_{DD_{nom}}) \) and the depleted \( V_{DD} \), and \( \Delta GND = \Delta V_{SS} \) is the difference between the elevated ground and \( V_{SS} = 0 \, V \).

![Fig. 1. 77-inverter chain ended by a level-sensitive D-FF, with variable \( V_{DD} \) (voltage ramp): (a) CDC=50%; (b) CDC=80%.
](image)

In Figure 1, SPICE simulation results obtained with a 77-inverter chain (to mimic a long signal path) designed in 130nm UMC CMOS technology (\( V_{DD_{nom}} = 1.2 \, V \)) illustrates \( V_{DD} - V_{SS} \) variation effects on circuit timing. The
clock period is $t_{CLK} = 1$ GHz$^1$. This figure highlights the *de-synchronization effect* when a signal path is ended by a level-sensitive D-type flip-flop (D-FF). Fig. 1(a) shows that the instant of de-synchronization ($t=31$ns) occurs for $V_{DD} = 0.98$ V; hence, the circuit functional collapse occurs at $83.33\%$ of $V_{DDnom}$ ($\gamma(vdd) = 16.67\%$), with CDC = 50%. In Fig. 1(b), the clock duty cycle is increased to CDC = 80%. The instant of de-synchronization ($t=40$ns) occurs for $V_{DD} = 0.88$ V. Now, the circuit functional collapse arises only at $73.33\%$ of $V_{DDnom}$ ($\gamma(vdd) = 26.67\%$). Thus, by increasing CDC, the circuit has been rendered more robust to the considered power interconnect noise.

The propagation delay caused by $V_{DD}-V_{SS}$ reduction, $T_{pd}(V_{DD})$, was previously analyzed and computed. A simple analytical model to predict the propagation delay variations in digital circuits, as a function of $V_{DD}$ variations has been proposed in [6][7]. This model can be used to compute the CDC stretching needed for a given power-supply oscillation.

### 3. METHODOLOGY FOR CDC MODULATION

The proposed methodology is based on the following assumptions:

**a)** CDC is generally set at 50% to minimize the *jitter effect* and the effects of parameters *spread* due to process variations; and to allow a *weighted-time distribution* for circuits designed with both rise- and fall-edge triggered flip-flops.

**b)** The maximum (minimum) value to which CDC can be stretched (shrunk) is significantly lower (higher) than 100% (0%), otherwise the combinational logic part collapses. The maximum (minimum) values depend on the application circuit, particularly on the propagation delays of the paths starting on the controlled flip-flops and on the flip-flops setup and hold requirements;

**c)** CDC may be temporarily modified for some functional parts of a SoC, but maintained unchanged for the other parts. This does not result in circuit functional error if the overall clock rate is kept unchanged and all the combinational parts of the circuit keep working synchronously.

In order to implement the proposed methodology, on-chip CDCM modules are added. Locally, CDCM modules monitor $V_{DD}-V_{SS}$ variations and modify the CDC accordingly. The power grid architecture and distribution to the different cores or SoC modules, determines how many CDCM modules should be inserted. Here, the methodology is illustrated using one power grid partition, one functional module and one CDCM module.

![Fig. 2. Basic architecture of the CDCM module.](image)

Fig. 2 represents the basic architecture of the CDCM module, comprising one CSL block which should introduce a minimum added clock delay. The clock signal provided by the CSL block feeds the circuit logic. The

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$^1$ Simulations have been carried out assuming that the clock signal goes on-chip through a buffer (two inverters), prior to trigger the D-FF.
CLS clock signal is synchronous with the PLL and it exhibits the same frequency. It will have a minimum stretch at nominal $V_{DD}$ (CDC slightly greater than 50%) and increases accordingly when $V_{DD}$ decreases.

![Diagram](image1)

**Fig. 3.** Typical architectures for: (a) CSL$_{up}$ and (b) CSL$_{down}$ blocks.

In Fig. 3, possible implementations of positive-edge (a) and negative-edge (b) CSL blocks using CMOS technology are shown. The main purpose of CSL is to increase CDC, in order to delay the (positive or negative) active edge of the clock, allowing the memory cells driven by this modified clock signal to capture the error free data. Positive (Negative) edge CSL delay $L \rightarrow H$ ($H \rightarrow L$) switching transitions. The M1-M2 inverter implements the CDC modulator core. M3, the pull-up PMOS transistor guarantees a slow driving capability. The result is a new modulated clock signal, with the same clock period, but with enhanced CDC in the presence of a reduction of $V_{DD}-V_{SS}$. The output signal can be buffered if needed. The two versions of the CSL (CSL$_{up}$ and CSL$_{down}$) are to be connected to rising (and falling)-edge activation flip-flops.

![Diagram](image2)

**Fig. 4.** CSL robustness to supply voltage variations: CSL output as a function of $V_{DD}$ decrease @ 200MHz; (a) CSL$_{down}$; (b) CSL$_{up}$.

Simulation results depicted in Fig. 4 (AMS 350 nm CMOS technology) show the CSL block capability to stretch (shrink) CDC proportionally to the depletion of $V_{DD}$. In Fig. 4(a), for CSL$_{down}$, different stretched CDC corresponding to several $V_{DD}$ values, from nominal $V_{DD}$ (3.3 V) to $V_{DD} = 1.2$ V can be observed. Note that the stretched CDC is always larger than 50% (the original duty-cycle), and lower than 100%. When $V_{DD}$ is depleted to the lowest possible value, 1.4V in Figs. 4(a), CDC reaches 82%. Beyond these values, the correct functionality collapses. In Fig. 4(b), the simulation results obtained for the rise-edge version of the CSL block (CSL$_{up}$), show a
CDC that decreases when VDD decreases until a minimum of 21%, with a VDD of 1.1V.

3.1 CDC STRETCHING MODEL

A model to accurately quantify CDC stretching as a function of VDD / VSS fluctuations has been developed. The amount of CDC variation, required to tolerate a given VDD disturbance, depends on the designer’s defined time slack value, tPM. Typically, it may correspond, for nominal values of the circuit parameters, to 8-10% of Tpd, the time period required by the longest critical path to propagate the switching values. When the power supply range, (VDD - VSS) decreases, it erodes tPM. One part of the speed degradation may be “absorbed” by the reduction in tPM, without causing a functional error; however, if this occurs, there is no guarantee of correct functionality. Therefore, in our approach, CDC variation, required to tolerate VDD variation, must preserve the nominal tPM value. If tCLK is the clock signal period, then

\[ t_{CLK} = T_{pd} + t_{PM} \]

In the absence of CDC modulation, CDC=50% and thus

\[ CDC = \frac{T_{on}}{t_{CLK}} = 50\% \]

where T_on is the time interval in which the clock signal assumes the ‘1’ logic value. When a ΔVDD occurs, a new value of CDC, referred as CDC’, must be applied. In the worst-case situation (for which nominal tPM is kept), CDC must stretch by the same amount of time required for signal propagation through the logic path. Hence,

\[ CDC' = \frac{T_{on} + T_{pd} \cdot \Delta T_{pd}}{t_{CLK}} \]

and

\[ \Delta CDC (VDD) = CDC' - CDC = \frac{T_{pd}}{t_{CLK}} \cdot \Delta T_{pd}(VDD) \]

As a consequence, CDC maximum variation follows Tpd(VDD) variation. The authors have previously proposed a simple analytical model [6][7] for this delay variation. The typical architectures of the CSL blocks, depicted in Figure 3, allow deriving such variation.

3.2 APPLICATION EXAMPLES

In this section some applications that prove the usefulness of the proposed methodology are presented. The methodology is applied to sequential circuits, particularly, to pipeline structures, and finite state machines (FSM). However, the methodology has some limitations, two generic and two particular to specific circuits.

The first generic limitation is the fact that the range of allowable correction of the CDC has its own limits. Consequently, the range of ΔVdd or ΔVss values for which signal integrity may hold is limited too.

The second generic limitation is associated with the presence of short paths. In fact, the use of a delayed clock edge trigger in a memory element raises the possibility that a short path in its input combinational logic cone will corrupt the data in the memory element. To prevent this corruption, a minimum-path length constraint is added at the input of each CDC controlled flip-flop in the design. As done in other design solutions [15], this limitation is solved by adding buffers to slow down fast paths. The minimum-path constraint is equal to the clock edge trigger
delay of the new CSL clock plus the propagation delay of the CSL block, that is:

\[
\min t_{pd} = |CDC_{clock} - CDC_{CSL}| \times T + t_{pdCSL} 
\]

The first specific limitation regards pipeline circuits. In this case, if a critical path is followed by another critical path in the following pipeline stage, the methodology still applies. However, the margin of application is now fixed by the addition of the two critical delays. This corresponds to smaller margin for \( \Delta V_{DD} \) and \( \Delta V_{ss} \). In some cases, the methodology can be applied using different CSL blocks for different memory cells.

The second specific limitation regards FSM. For some topologies the proposed methodology cannot be applied inside the FSM, namely, when combinational critical paths occur between the output and the input of feedback memory cells. Such particular loops will make the circuit insensitive to CDC variations.

### 3.3 Procedures to Improve Signal Integrity

In this section the procedures to implement the propose methodology are summarized. First, the following basic rules apply:

1. Identify, in the power grid, power supply blocks, presumably exposed to different power supply disturbances and physically disconnectable;
2. Use at least one CSL block for each power supply block;
3. Identify all critical paths;
4. All primary outputs of the circuit coming from combinational critical paths should be terminated with registers activated by CSL structures;
5. All primary inputs of the circuit connected to critical external blocks should be terminated with registers activated by CSL structures;
6. All registers that terminate critical paths must be activated by CSL structures;
7. All paths in the input combinational logic cones of a CDC controlled Flip-flop must meet the minimum-path constraint \((|CDC_{clock} - CDC_{CSL}| \times T + t_{pdCSL})\); otherwise, buffers should be added to increase the path delay to the minimum value;
8. Different CSL blocks with different CDC controls must be used for each critical path terminated register in continuous critical paths (connected through registers) in pipeline structures;
9. The method is not applicable in continuous critical paths (connected through registers) in a loop.

Although these basic rules generalize the application of the proposed methodology, they require a good knowledge of the circuit. However, one still can use it when this knowledge is limited. The CSL block can be used at least one for each module and power supply. It is also a good rule to make all primary outputs registered. If the methodology is not applicable (rule 9), but incidentally (e.g., if it is carried out in an automatic way) is applied, the system performance will not be degraded.

### 4. Experimental Results

The following results have been obtained with extensive SPICE electrical-level simulations under the Cadence framework and with CMOS AMS 350 nm technology. In the pipeline circuit of fig. 5, memory cells are rise edge
triggered type. In the FSM example depicted in fig. 7, memory cells are both rise and fall edge triggered types. In fig. 5(a) the pipeline structure has 2 memory cells (7 combinational logic gates), 4 inputs and 1 output. All critical path candidates end up in the Q2 memory cell. Hence, a CDCM is added to control the Q2 clock (fig. 5(b)), turning out Q2 flip-flop tolerant to the clock edge trigger.

![Fig. 5. Pipeline circuit example: (a) basic circuit; (b) with CSL block modulating the clock signal applied to Q2.](image1)

![Fig. 6. SPICE results for the Pipeline circuit example: (a) Without the CDCM system (Normal functionality, Vdd decreasing, Functional failure); (b) With CDCM system (CSL corrected clock, Functionality corrected, CSL clock and normal clock zoom).](image2)

Figure 6 shows SPICE simulation results for the Pipeline circuit example using pseudo-random vectors. Flip-flops are fall-edge trigger actives. The upper waveform in Fig. 6(a) shows the correct operation of Q2 (combinational critical paths). In the second waveform a $V_{DD}$ disturbance is modeled with a voltage ramp down and up. The lower waveform shows the functional error at Q2, caused by the disturbed $V_{DD}$. Introducing the CSL block (fig 5(b)) the problem is corrected. Thus, the upper waveform of fig. 6(b) shows the clock signal generated by CSL and applied to Q2. The second waveform shows the Q2 corrected functionality, proving that the delayed clock allows Q2 to capture the correct value during $V_{DD}$ depletion. In the lower waveform a zoom of the normal clock and of the CSL generated clock are shown, highlighting the CDC stretching, during VDD depletion.

The use of the methodology in circuits with both activating edges of the clock follows the same principle. However, the critical delay is now limited by half the clock period ($T/2$).

The second example, a FSM circuit (fig. 7(a)), has 4 memory cells, 4 inputs and 3 outputs and 17 combinational logic gates. This circuit has been stimulated with pseudo-random vectors, generated in the fall-edge of the clock. The circuit has 2 flip-flops with fall-edge trigger activation and 2 with rise-edge trigger activation. Now, the critical combinational paths of the circuit end at flip-flop Q3 (rise-edge trigger active), and
with a lower $V_{DD}$ this cell will capture the wrong signal value. Figure 8 shows SPICE results for the FSM circuit example. In the upper waveform of fig. 8(a) the correct operation of Q3 is shown. The second waveform shows the $V_{DD}$ disturbance (voltage ramp down and up). The lower waveform shows the erroneous Q3 signal, caused by $V_{DD}$. Introducing the CSL block (fig. 7(b)), the upper waveform in fig. 8(b) shows the clock signal modulated by CSL and applied to Q3. The second waveform shows a corrected functionality in Q3, demonstrating that the delayed clock allows the Q3 tolerance to $V_{DD}$ depletion. In the lower waveform a zoom of the normal clock and of the CSL generated clock are shown, highlighting the CDC shrinking, during VDD depletion.

Fig. 7. FSM circuit example: (a) basic circuit; (b) with CSL block modulating the clock signal applied to Q3.

Fig. 8. SPICE results for the FSM circuit example: (a) Without CDCM (Normal functionality, $V_{DD}$ decreasing, Functional failure); (b) With CDCM (CSL corrected clock, Functionality corrected, CSL clock and normal clock zoom).

5. CONCLUSIONS

A new methodology to enhance SoC signal integrity, by increasing circuit tolerance to $V_{DD}$ fluctuations is proposed in this paper. The goal is to keep circuit synchronism and performance (i.e., to keep at-speed operation) even in the presence of $V_{DD}$/GND disturbances that, by modifying propagation delays, may originate desynchronism.

The methodology is based on CDC modulation. The basic structure is the CSL block. In the worst-case situation, for which the stretched CDC keeps the user’s defined time slack, CDC variation is a replica of the propagation delay variation along the critical paths. The proposed methodology can deal with both positive and negative edge data capturing. The solution to the dual edge problem may be to use one CSL block (CSL$_{up}$) to
delay the positive edge of the clock signal, and another CSL block (CSL\textsubscript{down}) to delay the negative edge the clock signal. In digital circuits with dual edge trigger, not always (as shown in the FSM example) it is necessary to insert CSL\textsubscript{up} and CSL\textsubscript{down} blocks. Moreover, real time CDC adjustment allows time to correct (if necessary) the clock frequency without loosing data, when the IR V\textsubscript{DD} dropout is too severe.

Experimental results based on SPICE simulations demonstrate the effectiveness of the proposed methodology to detect abnormal V\textsubscript{DD}-V\textsubscript{SS} activity and to react to this disturbance by stretching the clock signal fed to the controlled logic. Simulation results have also shown the intrinsic robustness of the CSL block to the considered V\textsubscript{DD}-V\textsubscript{SS} transients. It is a primary condition that the CSL blocks must be, by design, more robust to V\textsubscript{DD}-V\textsubscript{SS} transients than the logic to be controlled. As shown in Section 3, Fig. 4, by carefully adjusting internal CSL blocks parameters it is possible to reach self-tolerance to power-supply oscillation up to 50%. It is worth noting that, as expected for any logic, this tolerance is operating frequency-dependent. The higher the frequency, the lower is the CLS tolerance to V\textsubscript{DD}-V\textsubscript{SS} oscillations.

As highlighted in Section 4, the implementation of the CDCM system to control clock edge trigger of some memory cells improves signal integrity in synchronous circuits and proves the validity of the proposed methodology and the usefulness of the proposed solution.

An additional problem associated with supply voltage variations occurs when a difference in supply voltage between a driver-receiver pair (in two physically separated logic blocks) creates an offset in the voltage with which the driver-receiver gates reference the signal transition. This has the effect of creating either a positive or a negative time shift in the perceived signal transition, at the receiver logic gate [16]. Work is in progress to extend the proposed methodology for such situations, and will be reported in the future.

REFERENCES


