Wireless Communication Systems For Intracortical Prosthesis


By INESC-ID

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Contributions to this report

This report includes written contributions and results of research work of: Prof. José Gerald, Prof. Moisés Piedade Engº Ricardo Ribeiro (PhD student). The report also includes work developed by the undergraduate students Pedro Cadima and Elísio Varela.

The reported work benefit with the helpful discussions in the periodical meetings realized within the SIPS research group, and within INESC-ID. Aiming the architecture implementation of the intracortical prosthesis in VLSI circuits, it includes the contribution of. Prof. Jorge Fernandes, Prof. Marcelino Santos, Liliana Pereira Ribeiro and Susana Gomes Pinto.

It also includes suggestions of Prof. Leonel de Sousa, Prof. Gonçalo Tavares, Profº Beatriz Borges, and Prof. Pedro Santos.

The work also benefited from the information of all CORTIVIS partners, in particular from the results of the Lisbon meeting (May the 22nd and 23rd 2003) of WP4 partners.
1. Introduction

This report concerns the work developed in the RF link in the context of CORTIVIS WP4 by INESC-ID in the project 2nd year. It describes the main activities and summarises the most relevant results. According to the planned, the work was oriented towards two goals: a discrete prototype and an integrated solution for the RF link. Most of the report respects to the former goal, but important results were achieved concerning the integrated solution, as described in sections 8 and 9.

The block diagram of the intracortical prosthesis system was already presented in deliverable D4 [1] and is shown in Fig.1.1. The system is divided in two parts: the primary and the secondary system. The former is located outside the human body and the later is designed to be placed inside the human body (not necessarily inside the head). Two radio frequency (RF) data links connect these systems: a forward link which transmits data from the primary to the secondary system and a backward link which operates in the reverse direction. For the discrete prototype half-duplex mode was considered.

For the discrete prototype, the forward link transmits a power/data signal modulating a carrier with a 1 MHz frequency. The data bit rate is up to 100 kbps using FSK (Frequency Shift Keying) modulation. After demodulation and frame disassembly, useful data is forward to the electrode stimulator.

The secondary power and main system clock are derived from the forward link signal. In the opposite direction DBPSK (Differential Binary Phase Shift Keying) will be used to modulate a 128 kHz carrier at a bit rate up to 16 kbps which suffices for maintenance purposes.

The coupling between the primary and the secondary system is done using a RF low coupling transformer.

This report concerns the work towards two products: a RF link prototype and a full “system on chip”. In the RF link, it was performed the optimizing, implementation in a PCB, and test of the theoretical architecture already chosen. This work is described in Chapters 2 to 6. In the fully integrated solution, work was made in the power recovery as well as in the electrode stimulation & control unit areas. This work is described in Chapters 7 to 9. The major conclusions and future work is presented in Chapter 10.
2. Primary System

2.1 System Architecture

The primary system architecture is shown in Fig. 2.1.

![Fig. 2.1 – Primary system architecture.](image)

This part includes an FSK modulator and a signal amplifier. The FSK modulator is implemented by means of a phase locked loop (PLL) drove by an oscillator at 1 MHz reference (carrier) signal. The amplifier is implemented by means of a class E tuned power amplifier.

The PLL diagram is represented in Fig. 2.2 and it is implemented by means of the IC HEF4046. The PLL parameter N (frequency divider) was made equal to one.

![Fig. 2.2 – PLL diagram of the FSK modulator.](image)

The chosen frequencies for the FSK modulation were 975 kHz and 1025 kHz. The loop filter has a pole at 10 kHz and a zero at 10 MHz. The PLL transfer function \( \omega_o/d\phi_o/dt \) is equivalent, in the frequencies under analysis, to a 2\(^{nd}\) order high pass filter one, with passband starting at around 20 kHz.
The class E switching-mode tuned power amplifier configuration was chosen to optimise the efficiency at the emitter [2]-[4].

2.2 Experimental Results

Figs. 2.3 to 2.6 show some of the experimental results obtained with the primary system emitter. Fig. 2.3 shows a square data signal and the corresponding VCO control signal at the emitter PLL.

![Fig. 2.3 - Square modulating signal and corresponding error signal](image)

Fig. 2.4 illustrates the PLL output FSK signal corresponding to the above mentioned data signal.

![Fig. 2.4 - FSK modulated signal](image)

Fig. 2.5 illustrates the transmission of the same data signal at several points of the class E tuned power amplifier and transformer.

A detail of the modulated signal spectrum at the secondary receiver input is shown in Fig. 2.6.

As one can see from Fig.s. 2.3 to 2.6, although an important attenuation is performed by the transformer, the information delivered to the secondary receiver is still a relevant one (to allow power and data recovery).
2.3 Conclusions

The designed circuitry, involving a PLL FSK modulator and a class E tuned power amplifier are adequate to transmit a sufficient and coherent 100 kb.p.s. signal through the chosen 1 MHz band, in spite of the transformer serious attenuation, resultant of its very weak magnetic coupling. The transformer design is described next.
3. Transformer

3.1 Parameters
In order to analyse the transformer behaviour, the classical equivalent circuit shown in Fig. 3.1 was used.

\[ L_{11} = L_1 - nL_M = L_1 - nk\sqrt{L_1L_2} = 30.27 \, \mu\text{H} \]
\[ L_M = k\sqrt{L_1L_2} = 5.41 \, \mu\text{H} \]
\[ L_{22} = L_2 - \frac{L_M}{n} = L_2 - \frac{k}{n}\sqrt{L_1L_2} = 26.73 \, \mu\text{H} \]

The loss capacitances \( c_{p1} \) and \( c_{p2} \) were neglectful. So, when operating at the series resonant frequency, the equivalent circuit can be replaced by that of Fig. 3.2.

3.2 Frequency Response

The simulation results shown next were obtained with the PSPICE circuit simulation program.
Figs. 3.3 to 3.5 illustrate the frequency response of the transformer for different magnetic coupling (different distances between both parts of the transformer) and different loads.

Fig. 3.3 – Transformer frequency response. a) Amplitude response. b) Phase response.
Fig. 3.4 - Transformer frequency response with varying load and k = 0.3. a) Amplitude response. b) Phase response. (RL=100 Ω, 200 Ω, 300 Ω, 500 Ω, 700 Ω, 900 Ω)(simulation).
The varying load frequency response was obtained for a distance of 0.5 cm (k=0.3) between primary and secondary coils.
This study aimed at the analysis of channel frequency response behaviour to a variable load which value would be around the expected value for secondary system power consumption (50 mW).
In both cases there is degradation in power transfer between primary and secondary, which is not significant to the load resistor values expected for the secondary system. In the first case degradation happens for lower load resistance, and in the second case for increased distance.

The filter distorts the magnitude and a phase of the signal because it has different gains and delays for different input signal harmonics in the interest bandwidth. The filter bandwidth is approximately 500 kHz, which allows the transmission bit rate required for this project (10 kbps to 100 kbps or even 1 Mbps).
Experimental results concerning the transformer frequency response are presented in Fig. 3.6. As one can see, in what respects to the resulting band pass, the obtained results do not agree with the previsions (simulation results). This fact will be discussed later, in section 3.4.

Fig. 3.6 – Transformer frequency response (experimental). a) Amplitude . b) Phase.
3.3 Efficiency

From the transformer simplified circuit (at the resonance frequency) of Fig. 3.2, with \( n=1 \), and considering an high inductor impedance at the resonant frequency, in order to evaluate the transformer efficiency, we can consider the following simplified circuit:

![Fig. 3.7 - Transformer simplified circuit at the resonant frequency.]

From the circuit presented in Fig. 3.7, we can obtain the following relations:

\[
P_{\text{OUT}} = \frac{V_{\text{OUT}}^2}{R_{\text{OUT}}} \quad \text{Eq. 3-1}
\]

\[
P_{\text{IN}} = \frac{V_{\text{IN}}^2}{R_{\text{Foss}} + R_1 + R_2 + R_{\text{OUT}}} \quad \text{Eq. 3-2}
\]

\[
\text{Eficiência} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} \quad \text{Eq. 3-3}
\]

\[
V_{\text{OUT}} = \frac{R_{\text{OUT}}}{R_{\text{Foss}} + R_1 + R_2 + R_{\text{OUT}}} V_{\text{IN}} \quad \text{Eq. 3-4}
\]

in which \( P_{\text{IN}} \) is the power supply delivered power and \( P_{\text{OUT}} \) is the power delivered to the load. From the above relations, considering that power supply impedance is null, one can obtain:

\[
\text{Eficiência} = \frac{R_{\text{OUT}}}{R_1 + R_2 + R_{\text{OUT}}} \quad \text{Eq. 3-5}
\]

Which is the maximum theoretical efficiency obtainable for the transformer.

As can be seen from Eq. 3-5, the transformer efficiency critically depends of the resistors \( R_1 \) e \( R_2 \) value, that is, larger values imply lower efficiency. One can conclude that the only way to increase transformer efficiency, keeping a fixed value for the load and for the operating frequency of the circuit, is to diminish inductor loss resistors, which might be accomplished by the manufacture of inductors using an isolated wire with some specific special characteristics.
From Eq. 3-5 and from the resistor values obtained for the resonance frequency to inductors $L_1$, $L_2$, $L_3$ e $L_4$, we obtain the efficiency plot depicted in Fig. 3.8.

![Transformer efficiency graph](image)

**Fig. 3.8 - Transformer efficiency measured for different values of resistances.**

### 3.4 Conclusions

After comparing the simulation results of the transformer with those of the experimental results, one can see that, in what concerns the frequency response, they are substantially different. This, in spite of the simulation and experimental results concerning both input and output impedances were identical. This can be explained by the fact that the transformer equivalent models used in literature consider always high magnetic coupling factors (parameter $k$ near 1) a model based on concentrated parameters in spite of being distributed. In fact, this is not the case here, where the absence of an iron core makes it impossible a strong magnetic coupling (the obtained coupling factor was 0.3). So, in order to increase the coupling factor, it were reduced the resistive losses in both the inductors by means of using a special multi-wire cable – Litz wire. The new results show that the transformer pass band is now around 1 MHz, as desired.
4. Secondary System

4.1 Receiver Architecture

The receiver architecture is depicted in Fig. 4.1.

One can see the 3 fundamental blocs: the power recovery, the data recovery and the clock recovery. The power recovery aims at obtaining 5 V DC in a stable way, from the received signal. The data recovery aims at demodulating the FSK signal and obtaining the transmitted data. The clock recovery aims at obtaining a 1 MHz reference clock for the local PSK emitter and received data synchronization. A more detailed circuit of the secondary receiver is shown in Fig. 4.2.
4.2 Data Recovery

Data recovery is accomplished by means of a PLL designed to perform an FSK demodulator. Experimental results of the data recovery processing are shown in Figs. 4.3 and 4.4. As one can see from these figures, scrambled data is properly transmitted and recovered at the receiver (the bit rate is 100 kb.p.s.).

![Fig. 4.3 – a) Emitted data. b) Corresponding PLL’s error signal at the receiver.](image1)

![Fig. 4.4 – a) Emitted data. b) Received data.](image2)

4.3 Clock Recovery

The clock recovery is accomplished by means of a PLL designed to produce a reference signal of 1 MHz from the received signal. Figs. 4.5 and 4.6 show experimental results obtained in several points of the clock circuitries, either at the emitter or the receiver.
Is particularly interesting to see in Fig. 4.6 the “degradation” (in what the clock recovery circuit is concerned) of the received signal, once it becomes modulated, as it is the usual situation.
4.4 Power Recovery

The local (secondary system) power supply 5 V DC is obtained by means of the circuitry shown in Fig. 4.7. It is composed of a half-wave rectifier, protecting circuits, and the IC LP298. A load resistance of 120 Ω was added whenever the clock recovery circuit was tested alone, to account for rest of the circuitry.

![Transformer output](image)

**Fig. 4.7 – Power recovery circuitry.**

Experimental results for emitter mid-charge 9 V battery are presented in Fig. 4.8, for several distances between both parts of the transformer.

![Graph](image)

**Fig. 4.8 - Experimental results for mid-charge battery.**

Experimental results for emitter mid-charge 9 V battery are presented in Fig. 4.8, for several distances between both parts of the transformer.

In what concerns the obtained efficiency with this system, Fig. 4.9 shows the experimental results for different distances between both parts of the transformer.
4.5 Conclusions

Although highly dependent from the distance between both parts of the transformer, for distances around 2 cm, all the receiver behaves properly, and a 5 V DC can be supplied to the receiver circuitry, as desired. Some problems are still persisting, but when the above mentioned distance get too short. This result in a very strong signal that can cause disturbances in the local PLLs. This problem is presently under resolution.

Fig. 4.9 – System power efficiency as a function of primary to secondary distance.
5. Secondary System Emitter (In/Out)

Using a very simple scramble polynomial:

\[ y(n) = x(n) \otimes y(n - 1) \]

and a simple PSK modulator, a very simple emitter was tested for inclusion in the secondary system. The choice of PSK was based on its robustness, relative insensitivity to amplitude errors and modulator simplicity. Fig. 5.1 illustrate the Matlab block diagram of the PSK modulator and experimental results obtained with discrete circuits operating alone.

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**Fig. 5.1 – PSK emitter.** a) block diagram (Matlab simulator); b) Emitted data; c) Modulated signal.
6. Prototypes

Figs. 6.1 to 6.3 illustrate the implemented prototypes of the emitter and receiver in PCB and transformer.

![PCB testing and transformer](image1)

*Fig. 6.1 – PCB testing and transformer.*

![Emitter PCB: a) Front; b) Rear](image2)

*Fig. 6.2 – Emitter PCB: a) Front; b) Rear.*

![Receiver PCB: a) Front; b) Rear](image3)

*Fig. 6.3 – Receiver PCB: a) Front; b) Rear.*
7. Data Communication Protocols, Formats and Digital Circuits

In the Lisbon meeting (May the 22nd and 23rd 2003), it was proposed by INESC a set of characteristics concerning the data communication protocols and others features, which was discussed by the WP4 partners. This set was generically approved by all partners. Next, the main conclusions for this set are referred.

7.1 Introduction

The goal here is to describe the communication protocol and the format used to transmit data through the RF link to the microelectrodes array stimulator. This is essential for the design of the data coder and decoder, located on the transmitter and receiver sides respectively, and the interfaces for these units. This document also discusses technical aspects of the digital circuits for data coding and decoding on both sides of the RF link and establishes the architecture of the digital micro-controller for the receiver part. The interfaces to D/A and A/D converters and to the artificial retina module, developed in WP2, are also presented.

7.2 Communication Protocol

From a communication perspective, the RF link is a serial transmission channel that may distort signals and introduce errors in the transmitted information. The transmission is asynchronous and a continuous flow of data maintains the communication channel busy. Dummy bits are sent whenever the artificial retina module does not provide any new information.

The selection of Address Event Representation (AER), without information about the event occurrence time and requirements for the receiver circuit, in regard to simplicity and power consumption, lead us to decision of not using any type of handshaking. A means for detecting errors will be provided but without auto-correction capacity. When errors occur, the incorrect information is discarded and no further action is taken. The inexistence of time stamps hardens other types of solutions and would lead to a much more complex receiver circuit.

7.3 Data Format

A stimulus for a microelectrode, designated by event, provides the 3 types of information presented in Table 7.1. It must be emphasized that no information is provided about time. It is assumed that the event is “instantaneously” communicated, which requires a communication system with low latency.
Information Length (bits)
Microelectrode address 10
Impulse amplitude 7
Impulse duration 5

Table 7.1: Information provided by the artificial retina for the stimulation of a microelectrode.

For serial RF transmission, the data is organized in packets with a pre-defined length, as depicted in Fig. 7.1. Each packet has 4 fields with a fixed length (HEADER, TYPE, VALID and CRC), a reserved bit and a data field (Event Data), which accommodates information about a pre-defined number of events. The number of bits is known both by the transmitter and the receiver.

**Header**

The header delimits a packet and synchronizes the communication. It is a pre-defined sequence of 10 bits that can never occur inside a data packet.

**Type**

The type field carries information about the type of event and the number of valid events presented in the packet. All the events in the packet are of the same type, and the 3 bits identify 8 different event types. This field is not completely specified, but the combinations already assigned are presented in Table 7.2: the stimulation event is used to stimulate a given microelectrode, while the measurement event requires the measurement of the state of a microelectrode to be known by the coder.

<table>
<thead>
<tr>
<th>TYPE bits</th>
<th>Event type</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Stimulation</td>
</tr>
<tr>
<td>001</td>
<td>Measurement</td>
</tr>
<tr>
<td>010</td>
<td>Undefined</td>
</tr>
<tr>
<td>011</td>
<td>Undefined</td>
</tr>
<tr>
<td>100</td>
<td>Undefined</td>
</tr>
<tr>
<td>101</td>
<td>Undefined</td>
</tr>
<tr>
<td>110</td>
<td>Undefined</td>
</tr>
<tr>
<td>111</td>
<td>Undefined</td>
</tr>
</tbody>
</table>

Table 7.2: Codes assigned to different event types.

**Reserved**

At this moment this bit is unused and should be equal to zero.

**Valid**
This 4 bit field represents the number of valid events in one packet, according to Table 7.3. The valid events are the first ones to appear in the packet. The dummy events that follow the valid ones are to be discarded by the receiver.

Not all events in a packet need to be valid. This is required when the retina model does not generate enough events to fill one packet. It is possible to have a packet without any valid event \(\text{Valid}=0\). This is useful in order to maintain the power supply to the receiver when there is no event available to transmit.

<table>
<thead>
<tr>
<th>Valid field value</th>
<th>4 event packet</th>
<th>8 event packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No event available</td>
<td></td>
</tr>
<tr>
<td>1 – 4</td>
<td>1 to 4 valid events</td>
<td></td>
</tr>
<tr>
<td>5 – 8</td>
<td>Unused</td>
<td>5 to 8 valid events</td>
</tr>
<tr>
<td>9 – 15</td>
<td>Unused</td>
<td></td>
</tr>
</tbody>
</table>

*Table 7.3: Valid field meaning.*

**Event**

Address and data corresponding to an event are represented with 22 bits, according to Table 7.1. A fixed number of events form a packet. This number is a tradeoff between the number of wasted bits to fill each packet and the percentage of useful bits in a packet. Two different numbers of events are considered, 4 and 8, depending on the number of microelectrodes. Based on the experiences made with the artificial retina module, these are reasonable numbers for arrays of 10x10 and 25x25 microelectrodes. However, its modification doesn’t change the general operation of the coding/decoding circuits. The percentage of useful bits for the setup with 4 and 8 events is 72% and 84%, respectively. It must be noted that the system is configured for one of the setups at the starting state and this configuration cannot be dynamically modified.

In Fig 7.1, bits from left to the right go from the header to the tail of the packet. It is also the order from the Most Significant Bit (MSB) to the Least Significant Bit (LSB), unless otherwise stated. The proposed order is defined to assure that the 10-bit HEADER combination never occurs twice in the packet. With this purpose, the coder identifies the repetition of the header in the packet and changes the value of the LSB. This change does not introduce a significant error, because it always occurs in the 2 LSBs of the fields.

**CRC**

A 16 bit Cyclic Redundancy Code (CRC) is appended to each packet. The following CRC generating polynomial is used:

\[
x^{16}+x^{12}+x^5+1
\]

Each time the CRC code detects an error the decoder circuit discards all data corresponding to the packet. It is a pragmatic solution justified by the conditions in which the system is operated.
22 x 8 (or 4) = 176 (or 88) bit

Fig. 7.1 – Data Format: a packet of bits.

### 7.4 Interface with the artificial retina module (WP2)

The artificial retina module generates events in an asynchronous way and the corresponding information is stored in a FIFO memory. Both circuits in Fig. 7.2 are operated in a synchronous way, which is achieved by using a common clock signal. The shared signals are referred in Table 7.4. RQS and ACK signals are used to implement a half-handshake communication protocol. The RQS signal is used to inform that there is data ready to send, but the transmission only starts after the ACK signal is set.

Fig. 7.2- Interface circuit to the artificial retina circuit (WP2-WP4).

<table>
<thead>
<tr>
<th>Signal</th>
<th>WP2</th>
<th>WP4</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_WP4</td>
<td>Input</td>
<td>Output</td>
<td>Clock</td>
</tr>
<tr>
<td>RQS</td>
<td>Output</td>
<td>Input</td>
<td>When active indicates that wp2 has events to transmit.</td>
</tr>
<tr>
<td>ACK</td>
<td>Input</td>
<td>Output</td>
<td>When active indicates that wp4 is ready to accept the events wp2 has to transmit.</td>
</tr>
<tr>
<td>DATA</td>
<td>Output</td>
<td>Input</td>
<td>Data bits.</td>
</tr>
</tbody>
</table>

Table 7.4 – Signal description
All signals are active high. **ACK** and **DATA** are synchronous to the rising edge of **CLK_WP4**. The **RQS** signal does not need to be synchronous.

One 22 bits long word of information is transmitted serially, starting from the address and from the MSB, according to the format depicted in Fig.7.3. This format, although similar, is not the same as the format chosen for an event in the RF-link communication protocol (see Fig.7.1). The bit order should be swapped by WP4, from one format to the other.

<table>
<thead>
<tr>
<th>Address</th>
<th>Amplitude</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB MSB</td>
<td>LSB MSB</td>
</tr>
<tr>
<td>10 bit</td>
<td>7 bit</td>
<td>5 bit</td>
</tr>
</tbody>
</table>

*Fig. 7.3 – DATA bits format for WP2-WP4 interface.*

![Temporal diagram of the interface signals (WP2-WP4).](image)

*Fig. 7.4 - Temporal diagram of the interface signals (WP2-WP4).*

Fig. 7.4 represents the temporal diagram for one transmission between WP2 and WP4. Initially both **RQS** and **ACK** are disabled and no communication is taking place. When WP2 has data ready to send, it asserts **RQS**. In response and when ready to receive the data, WP4 asserts the **ACK** signal (point A). WP4 circuits will read the first bit of data two clock cycles after asserting **ACK** (point B). The 22 data bits are serially transmitted, one bit per clock cycle. After the assertion of **ACK**, **RQS** should return to inactive level to which **ACK** will respond, going also to inactive level. In order to be possible to start a new transmission in burst mode, all this should happen before bit18 is read. The **RQS** signal should not be asserted again without **ACK** first returning to the inactive level.

The time it takes **ACK** to react to **RQS**, in case WP4 is ready to receive data, should be no longer than two clock cycles. When WP4 isn’t ready to receive data there is no limit to this response time.
A means to transmit several words in burst mode is provided, using the timing depicted in Fig. 7.5. The RQS signal is asserted before the end of the previous transmission. In order to guarantee that no delay occurs between the end of the previous word and the beginning of the next word, the RQS signal should be asserted in the clock transition corresponding to bit19 (point C). In that way, ACK should have enough time to respond to RQS, going active, in the transmission of the last bit (point D). Similar as before, the first data bit of the next transmission is output one clock cycle after and is read two clock cycles after (point E). Repeating this procedure, an uninterrupted transmission of several words is possible.

**7.5 Micro-controller and Electrode Stimulator**

Fig. 7.6 presents the block diagram of the micro-controller and the electrode stimulator. The serial data is de-scrambled in the data recovery block. The micro-controller separates the input data stream, identifies: a 10 bit address word and 12 bit of Data, and generates the Data Valid and Read control signals according to the type of event described in the TYPE field (see Fig. 7.1).

The 10-bit address identifies the target microelectrode. The 12-bit Data carries the amplitude and duration of the pulse to be applied to the microelectrode addresses. The amplitude is placed at the input of the DAC while the duration is stored in a register that works as a synchronous counter that maintains the amplitude valid during half the counting period and applies symmetric amplitude during the other half.
The Data Valid flag signals the Register array that the address and data buses have valid data. The Read flag signals the ADC to sense the signal being applied to the microelectrode. The 7-bit amplitude information and a Data Ready flag are sent back to the RF link in the opposite direction. The operating frequency of the ADC is not yet defined. However, it must be higher than the minimum pulse width to allow several samples during it.
8. Integrated Version of RF link - Power Recovery

8.1 Introduction

In the context of the CORTIVIS project, this work consists on the design of the power circuitry for the prosthesis. The main objectives are the optimization of the efficiency in the rectification and voltage stabilization stages, while keeping data integrity. Our preliminary experiments point to the fact that, when using transformers with low windings coupling, the power consumption is almost independent from the secondary load. Thus, the autonomy of the prothesys is not expected to be dependent of the rectifier and regulator circuits efficiency. However, efficiency is important in order to maximize the capability to deliver power to the active circuitry and also to minimize the aggression of local temperature changes.

The global circuit diagram is presented in Fig. 8.1.

![Block diagram of the prosthesis.](image)

The COSTIVIS project aims as much integration as possible of the prosthesis circuitry in order to minimize the corresponding impact and defect level. The AC/DC block is the only targeted in this work. The 3.3V output will supply the D/A converter, as represented in Fig. 8.1, and also the digital processing part, which is the one responsible for most of the power required from this voltage level. In fact the D/A block just needs to deliver a few microamps to the electrodes matrix, thus the 6.6V (that corresponds to the +3.3V in the matrix) rectification and regulation efficiency will not be attended with the same attention as the 3.3V. In fact, only the power required by the 3.3V (the specifications pointed to 108.9mW – corresponding to 3.3V in a 100Ω resistor) can justify extra hardware that can be used in order to increase efficiency.

This first part of the work consisted in the study of different rectification and regulation topologies, with the requirement of being suitable for implementation in integrated circuit with digital CMOS technology, with the transformer operating at 10MHz. Previous work taken into account in this study includes [5], [6], [7] e [8].
8.2 Rectifying Circuit

The transformer must work in resonant mode in order to minimize losses. The basic rectifier circuit used presented in Fig. 8.2. In this figure \( R_1 \) represents the resistive part of the transformer secondary winding and \( L_1 \) the inductance viewed from the same side. This is a simplified model that does not take into account all the transformer losses but was intentionally used in order to, realistically, enable the evaluation of the rectifying and regulation stages efficiency independently from the low magnetic coupling of the transformer.

![Fig. 8.2 – Rectifying circuit basic topology.](image)

\( C_1 \), being resonant with \( L_1 \), reduces the secondary impedance in the resonant frequency (10Mhz). The presence of this capacitor forces the transformer average current to zero. Thus, the diode \( D_2 \) is required in order to enable negative current flow of the same amount of positive current that passes through \( D_1 \). Notice that as \( R_L \) increases, the voltage in \( C_1 \) also increases and the current in both diodes decreases. In the limit this currents are zero and \( C_1 \) voltage equals the maximum value of \( v_1 \).

This topology is an alternative to a full wave rectification. In practice, full wave rectification requires two devices (diodes or transistors) in simultaneous conduction. Thus, in order to avoid a reduction in efficiency, larger devices would be required.

8.3 Voltage regulation

In order to be able to control the output voltage, a MOS transistor can replace either \( D_1 \) or \( D_2 \) in Fig. 8.2. Both solutions were analyzed.

If a MOS transistor is used in the position of \( D_2 \), it can be used to control the output voltage in two different ways:

1. By disabling the negative cycles of the current it limits the current in the positive cycles (since the average current in the capacitor \( C_1 \) is null). This type of control requires that, when maximum power transfer is
required, the MOS transistor be switched on every negative cycles of the current and switched off every positive cycle. This permanent switching would require a significant amount of energy since the MOS transistor must be large and consequently has a large capacitance associated to the gate that would be charged and discharged every cycle.

2. Using the MOS transistor in parallel with D2 and using it to shunt \( V_B \) to ground whenever the positive cycle of the current is not needed. This solution would give origin to large currents and voltages, and, depending on the windings coupling, eventually destroy the rectification and regulation circuit.

The adopted solution was regulating the output voltage using a PMOS transistor in the position of D1 (Fig. 8.2). The diode D2 is also implemented with a MOS transistor. The schematic of this solution is presented in Fig. 8.3.

In Fig. 8.3, transistor T2 implements diode D2 of Fig. 8.2, transistor T1 is used as a controlled switch to regulate the output voltage and transistor T3 is used to bias the well of T1, ensuring that this well is at the maximum input voltage, and thus disabling the parasitic diodes. These diodes inherent to the PMOS transistor implementation are represented in Fig. 8.4.
In Fig. 8.3, the capacitor C₃ represents the capacitance n-well/bulk that retains the peak voltage delivered by T₃. Note that this transistor gate is connected to its drain and not to ground in order to avoid the n-well discharge in the negative cycles of Vᵣ.

There are two ways to control the gate of T₁: linearly, with a constant voltage or, in an on/off approach, using a pulse. These two solutions need to be compared in terms of efficiency.

8.3.1 Linear voltage control

Fig. 8.5 shows the schematic of the circuit that allows regulation of the output voltage throughout the selection of a constant gate voltage for transistor T₁. This circuit was simulated using, the Spectre simulator in the Cadence “analog artist” environment, the AMS 0.35µm CMOS technology for different loads: Rₐ=100Ω, 200Ω, 300Ω e 1000Ω. For each load, the gate voltage of T₁ was selected to achieve 3.3V at V₄.

![Fig. 8.5 – Voltage regulation using a constant gate voltage in T₁.](image)

Fig. 8.6 shows an example of the voltages for the load 100Ω (Vᵣ is node 77, Vₚ is node 15 and V₄ is node 31)
Fig. 8.6 – Simulation of the regulation in linear mode.

The results of these simulations are summarized in Table 8.1.

<table>
<thead>
<tr>
<th>RL [Ohm]</th>
<th>VDC [V]</th>
<th>V0 [V]</th>
<th>Ron [Ohm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>0,00</td>
<td>4,030</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4,70</td>
<td>3,600</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4,90</td>
<td>3,330</td>
<td>55</td>
</tr>
<tr>
<td>200</td>
<td>5,90</td>
<td>3,600</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6,00</td>
<td>3,399</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>6,1</td>
<td>3,191</td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>6,0</td>
<td>4,401</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6,4</td>
<td>3,421</td>
<td>178</td>
</tr>
<tr>
<td></td>
<td>6,5</td>
<td>3,185</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td>7,0</td>
<td>3,652</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7,1</td>
<td>3,427</td>
<td>923</td>
</tr>
<tr>
<td></td>
<td>7,2</td>
<td>3,239</td>
<td></td>
</tr>
</tbody>
</table>

Table 8.1- Voltage regulation in linear mode.

8.3.1.1 Efficiency

The efficiency (η) was calculated as:

\[
\eta = \frac{P_{\text{load}}}{P_{\text{sup,ply}}} \times 100 \quad [\%] \tag{8.1}
\]

and since we have a constant voltage in the load:

\[
P_{\text{load}} = \frac{V_0^2}{R_L} \quad [W] \tag{8.2}
\]

The power delivered to the rectification circuit is:
Power loss in the rectification and regulation is given by:

\[ P_{\text{diss}} = P_{\text{sup plv}} - P_{\text{load}} \quad \text{[W]} \quad (8.4) \]

Table 8.2 shows the efficiency of the linear regulator circuit for different loads. The low efficiency values (<40%) obtained using this linear regulation approach lead to an attempt to perform regulation using MOS transistors working in less resistive conditions: the pulsed control.

### 8.3.2 Pulsed voltage control

Fig. 8.7 shows the schematic of the circuit that allows regulation of the output voltage pulsing the gate voltage of transistor T1, turning this device off or minimizing its drain-source resistance.

The regulation of the output voltage is carried out by turning T1 on n1 cycles in n2. The relative number of cycles that T1 is on is denoted by D=n1/n2.

The simulation results of the regulation circuit with pulsed control are presented in Table 8.3 for different loads.
Fig. 8.7 – Pulsed control regulation circuit.

<table>
<thead>
<tr>
<th>RL [Ω]</th>
<th>D</th>
<th>Period [ns]</th>
<th>Pulsed width [ns]</th>
<th>V0 [V]</th>
<th>Ron [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>4,5/5</td>
<td>500</td>
<td>423</td>
<td>3,057</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4,7/5</td>
<td>500</td>
<td>433</td>
<td>3,324</td>
<td>41</td>
</tr>
<tr>
<td></td>
<td>4,8/5</td>
<td>500</td>
<td>435</td>
<td>3,419</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>2,5/4</td>
<td>400</td>
<td>223</td>
<td>2,693</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2,8/4</td>
<td>400</td>
<td>240</td>
<td>3,344</td>
<td>54</td>
</tr>
<tr>
<td></td>
<td>3/4</td>
<td>400</td>
<td>298</td>
<td>3,764</td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>2,6/5</td>
<td>500</td>
<td>230</td>
<td>3,120</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2,7/5</td>
<td>500</td>
<td>235</td>
<td>3,327</td>
<td>62</td>
</tr>
<tr>
<td>1000</td>
<td>2,8/5</td>
<td>500</td>
<td>240</td>
<td>3,610</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1/5</td>
<td>500</td>
<td>98</td>
<td>3,496</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1,3/5</td>
<td>500</td>
<td>115</td>
<td>3,442</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1/6</td>
<td>600</td>
<td>98</td>
<td>3,300</td>
<td>79</td>
</tr>
</tbody>
</table>

Table 8.3 – Simulation results of the pulsed control circuit.

Fig. 8.8 shows the voltages wave forms when D=3/4 for a 100Ω load. (Vf is node 77, Vp is node 15 and Vd is node 31)
3.2.1 Efficiency

Table 8.4 shows the efficiency of the pulse-controlled regulator for different loads.

<table>
<thead>
<tr>
<th>$R_L$ [Ω]</th>
<th>$P_{carga}$ [mW]</th>
<th>$P_{gerador}$ [mW]</th>
<th>$P_{dissipada}$ [mW]</th>
<th>Rendimento [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>110,49</td>
<td>331,80</td>
<td>221,31</td>
<td>33,30</td>
</tr>
<tr>
<td>200</td>
<td>55,91</td>
<td>165,30</td>
<td>109,39</td>
<td>33,82</td>
</tr>
<tr>
<td>300</td>
<td>36,90</td>
<td>115,80</td>
<td>78,90</td>
<td>31,86</td>
</tr>
<tr>
<td>1000</td>
<td>10,89</td>
<td>38,05</td>
<td>27,16</td>
<td>28,62</td>
</tr>
</tbody>
</table>

Table 8.4 – Efficiency of the pulsed regulator for different loads.

8.3.3 Analysis of the efficiencies of the linear and pulsed regulators

Based on the results presented in the previous sections, Fig. 8.9 compares the efficiency of both schemes of voltage regulation. The efficiency values are similar and the linear regulator always exhibits higher values than the pulsed one. The reason for this difference is not the power lost in T1. In this transistor the power is the same in both regulators since the decrease in resistance is associated with an increase in the RMS value of the transistor current that results in the same power loss in the device. However, the increase in the RMS current value is responsible for additional losses in the other resistive elements of the circuit (R1). This analysis is demonstrated in the following paragraphs.
Using the Kirchhoff’s laws for average values [9] we can easily conclude that the average value of the load and transistor T1 currents is the same in both types of regulation:

\[ \bar{i}_{\text{VDC}} = \bar{i}_{\text{VPulse}} \]  \hspace{1cm} (8.5)

With linear regulation, the average current in the source of T1 is:

\[ \bar{i}_{\text{VDC}} = \frac{1}{T} \int_0^T i(t) \, dt = \frac{1}{2\pi} \int_0^{2\pi} I_{M_{\text{VDC}}} \text{sen}(\sigma_0 t) \, dt = \frac{I_{M_{\text{VDC}}}}{\pi} \]  \hspace{1cm} [A]  \hspace{1cm} (8.6)

With the pulsed regulator the current through T1 can be defined as:

\[ i_p(t) = \begin{cases} I_{M_{\text{VPulse}}} \text{sen}(\sigma_0 t) & , \text{sen}(\omega_0 t) > 0 \wedge V_P=1 \\ 0 & , \text{sen}(\omega_0 t) < 0 \vee V_P=0 \end{cases} \]  \hspace{1cm} [A]  \hspace{1cm} (8.7)

where \( V_P \) denotes the control voltage applied to the gate of T1 and \( I_{M_{\text{VPulse}}} \) is the maximum value of the current. The average value of this current is:

\[ \bar{i}_{\text{VPULSE}} = \frac{1}{T} \int_0^T i(t) \, dt = D \frac{I_{M_{\text{VPULSE}}}}{\pi} \]  \hspace{1cm} [A]  \hspace{1cm} (8.8)

where D, as previously defined, is the ratio of used cycles (T1 “on” \( n_1 \) cycles in each \( n_2 \) cycles):

\[ D = \frac{n_1}{n_2} \]  \hspace{1cm} (8.9)

Taking into account (8.5), (8.6) and (8.8), we can obtain:

\[ \bar{i}_{\text{VDC}} = \bar{i}_{\text{VPULSE}} \iff \frac{I_{M_{\text{VDC}}}}{\pi} = D \frac{I_{M_{\text{VPULSE}}}}{\pi} \iff I_{M_{\text{VPULSE}}} = \frac{I_{M_{\text{VDC}}}}{D} \]  \hspace{1cm} (8.10)

Using a linear model for the resistance of T1 (\( R_{\text{on}} \) always present in the linear regulator, \( R_{\text{on}} \) present when T1 is “on” for the pulsed regulator), the corresponding values of \( R_{\text{on}} \) can be obtained using expression (8.11) for the linear regulator and using

![Figure 8.9 – Efficiency of the linear and the pulsed regulators.](image-url)
expression (8.12) for the pulsed regulator. These expressions are valid for the maximum values of the currents.

\[ Ron_{VDC} = \frac{V_f - V_d}{I_{M_{VDC}}} \quad [\Omega] \quad (8.11) \]

\[ Ron_{PULSE} = \frac{V_f - V_d}{I_{M_{PULSE}}} \quad [\Omega] \quad (8.12) \]

Using (8.10) and (8.12) we can compare the values of \( R_{on} \) for both types of regulation:

\[ Ron_{PULSE} = \frac{V_f - V_d}{I_{M_{PULSE}}} = \frac{V_f - V_d}{I_{M_{VDC}}} = \frac{V_f - V_d}{D} = Ron_{VDC}.D \quad [\Omega] \quad (8.13) \]

that is, \( R_{on} \) with pulsed control is reduced by a factor of \( D \), when compared with the linear regulator.

In both types of regulation, the power losses in T1 are approximated by:

\[ P = I_{rms}^2 . Ron \quad [\text{W}] \quad (8.14) \]

where:

\[ I_{rms} = \sqrt{\frac{1}{T} \int_0^T i(t)^2 dt} \quad [\text{A}] \quad (8.15) \]

For the linear regulator, the RMS value of the current is:

\[ I_{rms_{VDC}} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} T^2_{M_{VDC}} \text{sen}^2(\theta) d\theta} = \sqrt{\frac{I_{M_{VDC}}^2}{2\pi} \frac{1}{2} \int_0^{\pi} \frac{1}{2} [1 - \cos(2\theta)] d\theta} \leftrightarrow \]

\[ \Rightarrow I_{rms_{VDC}} = \frac{I_{M_{VDC}}}{\sqrt{2\pi}} \int_0^{\pi} \left[ \frac{1}{2} (\theta - \text{sen} \theta \cos \theta) \right] d\theta = \frac{I_{M_{VDC}}}{\sqrt{2\pi}} \int_0^{\pi} \frac{1}{2} (\pi) \leftrightarrow \]

\[ \Rightarrow I_{e_{VDC}} = \frac{I_{M_{VDC}}}{2} \quad [\text{A}] \quad (8.16) \]

and the power losses in T1 are:

\[ P_{VDC} = I_{rms_{VDC}}^2 . Ron_{VDC} = \left( \frac{I_{M_{VDC}}}{2} \right)^2 . Ron_{VDC} = \frac{I_{M_{VDC}}^2}{4} . Ron_{VDC} \quad [\text{W}] \quad (8.17) \]

The RMS current in the pulsed regulator is:

\[ I_{rms_{PULSE}} = \sqrt{\frac{D}{2\pi} \int_0^{\pi} I_{M_{PULSE}}^2 \text{sen}^2(\theta)^2 d\theta} \leftrightarrow \]
\[ I_{\text{rms}_{-}\text{PULSE}} = \frac{I_{M_{-}\text{PULSE}}}{{\sqrt{D}}} = \frac{I_{M_{-}\text{VDC}}}{{\sqrt{D}}} \] [A] \hspace{1cm} (8.18)

and the corresponding power losses in T1 are:

\[ P_{\text{VPULSE}} = I^2_{\text{rms}_{-}\text{PULSE}} \cdot R_{\text{on}}_{\text{VPULSE}} = \left( \frac{I_{M_{-}\text{VPULSE}} \cdot {\sqrt{D}}}{{2}} \right)^2 \cdot R_{\text{on}}_{\text{VPULSE}} \]

\[ \Rightarrow P_{\text{VPULSE}} = \left( \frac{I^2_{M_{-}\text{VDC}}}{{2\sqrt{D}}} \right) \cdot R_{\text{on}}_{\text{VDC}} \cdot D = \frac{I^2_{M_{-}\text{VDC}}}{{4}} \cdot R_{\text{on}}_{\text{VDC}} \] [W] \hspace{1cm} (8.19)

The conclusion is that in the pulsed regulator the RMS current \( I_{\text{rms}_{-}\text{PULSE}} \) increases (by a factor of \( \frac{1}{{\sqrt{D}}} \)) and \( R_{\text{on}} \) is reduced by a factor of \( D \), resulting in the same power losses in T1.

### 8.4 Current work

In order to allow voltage regulation, using MOS transistors as switches with low \( R_{\text{on}} \), without increasing the values of the RMS current in the switch, an inductor \( L_2 \) was added. The schematic of the resulting circuit is presented in Fig. 8.10. \( L_2 \), \( C_4 \) and \( T_4 \) (acting as a diode) perform current filtering enabling low \( R_{\text{on}} \) with low value of T1 RMS current. \( L_2 \) will be external to the IC as well as \( C_3 \). This additional inductor will require a unique additional pad since one terminal of \( L_2 \) is common to \( C_3 \).

Fig. 8.11 shows the currents and voltages for the circuit of Fig. 8.10. This circuit is, at the moment, being designed with the CXZ 0.8\( \mu \)m high voltage technology from AMS. The selection of this technology was based on the simulated values of the voltages in all the circuit nodes. The preliminary results obtained with the schematic presented in Fig. 8.10 point to efficiency values above 75%.
Fig. 8.10 – Regulation using an output current filter.

Fig. 8.11 – Voltage at the source of T1 (net10), L2 current (x100) and output voltage for the circuit of Fig. 8.10.
9. Integrated Version - Electrodes Stimulator and Control Unit

9.1 Introduction

In this section we refer to the Electrodes Stimulator and Control blocks in the secondary system represented in Fig. 9.1.

The secondary system receives the information from the Primary System through an RF link. The data received is then processed and in the Data Processing block and sent to the Control and the Electrode Stimulator blocks. This module has three main sub-blocks: the addressing decoder (10:1024), the 1024 DACs matrix, and one ADC. The ADC is used to return the stimulus information to the primary system. The ADC is already under study in 2004 and we will not include it in this report.

A stimulus has three types of information:

1) Electrode Address – 10 bits
2) Impulse Duration – 5 bits
3) Impulse Amplitude – 7 bits

In Fig. 9.2 we represent a more detailed block diagram for the control unit and the electrode stimulator blocks. The transmission rate is 1 Mbit/s serial.

The addressing decoder has serial–to-parallel converters to store the three needed words: the Electrode Address, the Impulse Duration and the Impulse Amplitude. Then it activates just the selected pair DAC/Electrode and controls it.

The DAC is the most important block because we have chosen to have one 7 bit DAC for each electrodes implemented with a structure that ensures that ensures that the charge applied to the electrode is also removed from the brain once the electrode is stimulated.

The circuits were designed in AMS 0,35µm CMOS technology [10,11]. The DAC has 0,886 mW power consumption and the total area is 36,3 mm².

The supply available for these blocks is

- +3,3 V for the digital part (Power consumption < 200 mW)
- +10 V and –10 V for the electrodes (Current biasing < 1 mA)
9.2 System Architecture

In Fig. 9.3 we represent a more detailed block diagram where we can note that the 1024 DAC matrix is implemented in a $32 \times 32$ structure. Therefore the decoder has two 5 bit serial to parallel blocks to address the DAC. These decoders use PMOS transistors in a tree structure. Also, the control unit ensures that the DAC is enabled for the same period duration with the same amplitude while exciting the electrode or removing the charge from the brain.
Descodificador de endereço

Conversor série paralelo de 10 bits

10 bits em série (endereço do par DAC/eléctrodo)

Conversor série paralelo de 7 bits (amplitude)

7 bits em série (amplitude)

Conversor série paralelo de 5 bits (duração)

5 bits em série (duração)

Conversor série paralelo de 5 bits (duração)

7 bits em série (amplitude)

5 bits em paralelo (duração)

Sinal que desactiva o DAC

Sinal que desactiva o DAC

Duração positiva do sinal a enviar ao eléctrodo

Duração negativa do sinal a enviar ao eléctrodo

Fig. 9.3 - System architecture.
In Fig. 9.4 we represent the DAC control algorithm. This diagram converts the data from serial to parallel, activates the DAC and then the DAC plus its control logic is working standalone, i.e., the DAC has all the information to excite the electrode, remove the charge from the brain and turn itself off. This scheme is robust and if any DAC fails it only means that a electrode will be unavailable.:

In Fig. 9.5 we represent a more detailed block diagram of the decoder with 5 bit serial to parallel blocks to address the $32 \times 32$ matrix DAC. These decoders use PMOS transistors in a tree structure as represented in Fig. 9.6.
9.4 DAC

The DAC architecture is a current-steering type (Fig. 9.7). It uses scaled currents that add at the output node to ensure the desired linear digital-to-analog conversion. The main difference between the circuit in Fig. 9.7 and a common Current-steering DAC is
that the one in Fig. 9.7 allows for the removal of the charge from the brain. It means that it can inject current (positive sign) or remove current (negative sign) from the electrode.

The reference current is 24 μA, which leads to a $W = 90 \mu m$, $L = 0.35 \mu m$, for the reference transistor dimension. To implement the bits weight in the structure the equivalent dimensions of the transistors are (note. the implementation uses unit dimension transistors in parallel to do the weighting):

$I_1 \rightarrow b_1 \rightarrow W_{eq} = 2 \times 1.4 \mu m \rightarrow W_{eq} = 2.8 \mu m$

$I_2 \rightarrow b_2 \rightarrow W_{eq} = 4 \times 1.4 \mu m \rightarrow W_{eq} = 5.6 \mu m$

$I_3 \rightarrow b_3 \rightarrow W_{eq} = 8 \times 1.4 \mu m \rightarrow W_{eq} = 11.2 \mu m$

$I_4 \rightarrow b_4 \rightarrow W_{eq} = 16 \times 1.4 \mu m \rightarrow W_{eq} = 22.4 \mu m$

$I_5 \rightarrow b_5 \rightarrow W_{eq} = 32 \times 1.4 \mu m \rightarrow W_{eq} = 44.8 \mu m$

$I_6 \rightarrow b_6 \rightarrow W_{eq} = 64 \times 1.4 \mu m \rightarrow W_{eq} = 89.6 \mu m$

The output current is in average 14.88 μA, assuming a output resistance of 2 kΩ we have $\bar{P} = R \times \bar{I}^2 = 0.886$ mW. This is the average power consumption while working, it should be noted that when not addressed the DAC is off.

The correct functional behaviour of the system is represented in Fig. 9.8.

The transfer characteristics of the DAC are represented in Fig. 9.9.
Fig. 9.8 – DAC outputs for a full-scale transient analysis.

Fig. 9.9 – DAC transfer characteristic.

9.5 Layout

The technology used is 0.35μm CMOS from AMS (Austria Mikro Systeme Int) [10,11]. The DAC has 0.03 mm² (0.0695mm x 0.443 mm) and is represented in Fig. 9.10.
In Fig. 9.11 have the layout of the complete control unit with only 4 DAC mapped on just for area evaluation proposes. With 1024 DACs we can estimate an area of 36.3 mm$^2$ for the whole circuit.
Fig. 9.11 – System layout (only 4 DACS are represented).

Based on this work, a paper will be presented on ISCAS’04 [12].
10. Conclusions and Future Work

In the first year of this project, WP4 working group have focused his work on the RF link system architecture and the choice of basic options, such like the type of modulation used in the RF transmission, the basic structure of the RF tuned amplifier, and so on, as described in the deliverable report D4. Also, some studies were performed towards the goal of producing a system on chip.

In this second year, in what concerns the RF link, the work was to implement all the theoretical choices, optimise their functioning and test the implemented circuitry. This task was performed with the primary system emitter, the transformer and the secondary system receiver.

Among the several problems found, a major one was the transformer behaviour, which, because of its weak magnetic coupling, is somehow different from the models found in literature. The improvement of the coupling factor was achieved by means of using a multi-wire cable, Litz cable, in order to reduce the inductors losses.

An emitter/receiver prototype was produced in PCB. Also, some work began to be produced in the reverse-link, i.e. the secondary system emitter and the primary system receiver (transmission in/out). In the future, this facility will be available, and may be added to the forward-link prototype.

Concerning the full integrated solution, work was made in (i) the power recovering area, where the main objectives are the optimization of the efficiency in the rectification and voltage stabilization stages, while keeping data integrity, and in (ii) the electrodes stimulator and control unit.

In the power area, a circuit is being designed with the CXZ $0.8\mu m$ high voltage technology from AMS. Preliminary results point to efficiency values above 75%. Future work includes 6.6 V output. The 6.6V output of the power module will be obtained adding an additional transistor T5 as presented in Fig. 10.1. This output will be regulated using a constant gate voltage since the current requested from this output is very small. Additional topics are: Design of the control circuit for voltage regulation; layout design and Pos-layout simulation.

In the electrodes stimulator and control unit area, a DAC test circuit was produced, using the technology $0.35\mu m$ CMOS from AMS. The DAC has $0.03 \text{ mm}^2 (0.0695 \text{ mm} \times 0.443 \text{ mm})$. This circuit is under test. However, from the work presented in this report many conclusions towards the final prototype design have been taken.

- The technology should be AMS CMOS $0.8\mu m$ HV due to the voltage spikes in the transformer secondary.
- The modules should have a $10 \times 10$ Array with $4 \times 4 \text{ mm}^2$, Each chip should have only 100 DACs.
- The final prototype should be implemented in a Flip-chip over the electrode array, as shown in Fig. 10.2. Each electrode has $400\mu m \times 400\mu m$ area.
- The DAC’s should be revised and update to new technology.
- The Control unit should be revised and designed using VHDL for flexibility.
- The ADC should be implemented.
- The Electrode Buffer characteristics should be evaluated.
Figure 10.1 – Additional circuitry (T5) for 6.6V regulation.

Fig. 10.2 – System on chip stimulator&DAC.
Bibliography


