Using Variable $V_{DD}$ for Delay Fault Detection and Tolerance Improvement in CMOS Digital Systems

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Dissertation for obtaining the Master degree in

Engenharía Electrotécnica e de Computadores

Jury

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September, 2008
Acknowledgements

I would like to thank to Professors João Paulo Teixeira and Isabel Teixeira for all the support, encouragement and guidance during this work and through the past four years.

I would also like to thank to Professor Marcelino Santos all the support, motivation and precious advices.

I am extremely thankful to Jorge Semião for all the support, motivation, advices, available time and help during the last months.

Finally, I would like to thank to my family and to Tiago Saraiva for their love, support, encouragement and patience.
Abstract

Electronic design of high-performance digital integrated systems in nanometer technologies, taking into account area, performance, power consumption, and quality requirements, is a challenging process. New node technologies are more sensitive to process variations. Moreover, operation-dependent disturbances, namely due to power supply Voltage (V_{DD}) and Temperature (VT) variations, tend to modulate circuits timing response, which may induce logic errors (due to data capture in inadequate time frames), or compromise the test process, targeting delay fault detection. Sensitivity to PVT (Process, and VT) variations also increases with technology downscaling, as V_{DD} decreases and power density increases.

Recently, a novel VT-aware design methodology has been proposed, which leads to enhanced tolerance to VT variations, even in the presence of process variations, without compromising circuit performance or testability. The methodology, which uses the concept of dynamic time borrowing, has been demonstrated with ideal V_{DD} sources, feeding digital circuits operating in functional mode.

The purpose of this dissertation is twofold. First, to investigate the effects of non-ideal V_{DD} sources, due to non-ideal power grids in digital systems, on circuit performance. Second, to analyze the consequences of implementing the VT-aware methodology in digital circuits designed with DfT (Design for Testability) techniques, namely with scan. Extensive circuit-level simulation is used and a novel test set-up circuit, to emulate large designs, is proposed. The goal is to characterize the expected power supply noise effects (resistive and/or inductive parasitics) on timing response, and to find out if the proposed VT-aware methodology can still be applied, with non-ideal V_{DD} and with DfT.

As shown with combinational, pipeline and sequential circuits (industrial and benchmark), it is demonstrated that the VT-aware methodology can still be applied in the presence of non-ideal power supply voltage sources, although the amount of gained tolerance may depend on the voltage source non-ideality. Furthermore, it is shown, for the B06 ITC’99 benchmark circuit, that the dynamic time borrowing concept can still be used in multi-V_{DD} scan design, provided that special care is taken, as far as managing time borrowing in functional and in test modes of operation.

Keywords

Process Voltage and Temperature Variations; Power Supply Noise; Time Borrowing; Design & Test.
Resumo

O projecto de sistemas electrónicos de elevado desempenho, em tecnologias nanométricas, considerando requisitos de área, desempenho, consumo e qualidade é um desafio. Os novos nós tecnológicos são mais sensíveis a variações no processo de fabrico. Perturbações induzidas na operação, em particular devidas a variações da tensão de alimentação ($V_{DD}$) e da temperatura, modulam a resposta temporal dos circuitos, podendo causar erros lógicos ou comprometer o processo de teste. O escalonamento da tecnologia aumenta a sensibilidade a variações PVT (de processo, de tensão ($V_{DD}$) e de temperatura), à medida que tensões $V_{DD}$ menores são usadas e que a densidade de potência aumenta. Foi proposta recentemente uma metodologia de projecto sensível a variações de VT, que aumenta a tolerância a estas variações, mesmo na presença de variações do processo, sem comprometer o desempenho nem a testabilidade dos circuitos. A metodologia, que utiliza o conceito de empréstimo temporal dinámico, foi demonstrada com fontes de tensão ideais, alimentando circuitos digitais a operar no seu modo normal.

O objectivo desta dissertação é duplo. Primeiro, investigar os efeitos da não idealidade de fontes de tensão $V_{DD}$ no desempenho dos circuitos, resultante da não idealidade das redes de distribuição da alimentação no circuito integrado. Segundo, analisar as consequências de utilizar a metodologia VT em circuitos digitais projectados com técnicas de testabilidade, nomeadamente com auto-teste ou varrimento. Utiliza-se extensivamente o teste a nível eléctrico e propõe-se um novo circuito equivalente, para simular circuitos mais complexos e a não idealidade de $V_{DD}$. Caracterizam-se os efeitos de ruído na alimentação (resistivos e indutivos) na resposta temporal e averigua-se se a metodologia VT pode ainda ser utilizada com $V_{DD}$ não ideais e com técnicas de teste.

Utilizando circuitos combinatórios, em cascata e sequenciais (industriais, e de referência), prova-se que a metodologia VT pode ainda ser utilizada com $V_{DD}$ não ideais, embora os ganhos de tolerância dependam da não idealidade da fonte e da rede de alimentação. Para o circuito de referência B06, demonstra-se que o conceito de empréstimo temporal é válido num ambiente multi-$V_{DD}$ em circuitos com varrimento, operando em modo normal, ou de teste.

Palavras-Chave

Variações de Tensão e Temperatura; Ruído de Fonte de Tensão; Empréstimo Temporal; Desenho & Teste.
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List of Acronyms and Abbreviations

AMS – Austria Micro Systems™
ATPG – Automatic Tester Pattern Generator
BIST – Built-In Self-Test
BRI – Bridging defect (resistive)
CME – Critical Memory Elements
CMOS – Complementary MOS
CP – Critical Path
CUT – Circuit Under Test
DDB – Dynamic Delay Buffer
DPM – Defective Parts per Million
DVFS – Dynamic Voltage and Frequency Scaling
DUT – Device Under Test
DVS – Dynamic Voltage Scaling
DyDA – Dynamic Delay Analyser (software tool)
EDA – Electronic Design Automation
EMC – Electromagnetic Compatibility
EMI – Electromagnetic Interference
ESD – Electrostatic Discharge
FF – Flip-Flop
FM – Fault model
FSM – Finite State Machine
IC – Integrated Circuit
IP – Intellectual Property
LFSR – Linear Feedback Shift-Register
LOC – Launch on Capture
LOS – Launch on Shift
LP – Low-Power
LSA – Line Stuck-At (fault model)
MOS – Metal-Oxide-Semiconductor
MISR – Multiple Input Shift Register
ORA – Output Response Analyzer
PI – Primary Input
PLA – Programmable Logic Array
PO – Primary Output
PSN – Power Supply Noise
PVT – Process, power supply Voltage and Temperature (variations)
RTL – Register Transfer Level
SI – Secondary Input
SO – Secondary Output
SoC – System-on Chip
STA – Static Timing Analysis
TAE – Test Answer Evaluator
TB – Time Borrowing
TL – Test Length
TPG – Test Pattern Generator
VT - Power supply Voltage and Temperature (variations)
1. Introduction

New product development of electronic systems using nanometer IC (Integrated Circuit) technologies is facing many challenges. Every new node technology pushes further semiconductor technology down to its limits, requiring new processing materials and equipment and unveiling novel failure mechanisms, which must be detected during production test. Meanwhile functionality, performance, quality and cost requirements never cease to increase, while power consumption and silicon area per function requirements never cease to decrease. Electronic Design Automation (EDA) tools must support reliable, right-first-time design, which requires more and more sophisticated software tools. Moore’s law is expected to continue for the years to come, boosting economic growth. Nevertheless, power consumption, power density, energy budgets (in portable equipments) and thermal issues require ever decreasing power supply voltages, thus eroding noise margins. Moreover, the increase in lithographic resolution (MOS thin oxide gates are now composed of few atom layers, dopant atoms in MOS channel regions are now a discrete number) increases process variations and susceptibility to environmental or operation-dependant disturbances.

High performance applications, like digital System-on Chip (SoC) products and microprocessors, need to take advantage of all available dynamic performance of the physical devices, while maintaining signal integrity [1]. However, in order to take into consideration process, power supply voltage and thermal variations, a significant time slack needs to be introduced, in order to guarantee high production yield and, thus, profitability [2]. Time slack provides the safety margin to ensure performance specifications compliance: the design is carried out with nominal parameter values, the maximum clock frequencies (in a multi-clock domain design) are computed, and a time margin (time slack) is added to accommodate expected variations.

Assuming a fault-free die, the signal integrity problems in synchronous digital SoC may be caused by process variations or circuit operation. In the physical structure, signals may arrive too late or too early, which means that signals may be captured and transmitted in an incorrect time window [3]. If this happens, the behaviour of a fault free die is no longer correct as expected. Such incorrect behaviour may strongly depend on circuit operation. For instance, in production test, high fault coverage requires high switching activity (to check the entire physical structure). This means that test power (the power consumption in test mode) typically exceeds normal power. Overheating depends on the specific operation pattern, produces a variable thermal map (in time and space), which makes it difficult to predict the exact circuit behaviour. Consequently, the results of the test process may produce false positives (good dies identified as faulty) or negatives (defective parts that pass test, and are commercialized as good). In the first case, a yield loss may compromise profit; in the second case, product quality (and customer’s satisfaction) decreases, which may have disastrous consequences for business.

High-performance specs require limited time slacks. Operation-dependent parametric variations may cause performance variations, due to power supply noise (PSN) (or \( V_{DD} \) variation) and / or due to temperature variation [3]. PSN is a clear result of non-ideal power grids (the physical structures in the IC layout that distribute the power supply voltage along the chip), high power supply current pulses (during synchronous gate switching activity, at clock signal edges), and I/O chip circuitry and pins. Temperature variations are induced by power consumption, as it induces thermal variations including temperature gradients along the die. Often, to restrict power consumption, Low-Power (LP) design techniques are used, namely, Dynamic Voltage Scaling (DVS). If this is the case, multi-\( V_{DD} \) can be available on-chip, by means of a power management unit.
Power supply voltage and temperature variations can make signals to arrive too late or too soon at key nodes of the circuit [2]. Such timing-faults, not due to a physical defect, are operation-dependent. Nevertheless, they are just enough to make the system fail its performance and to be rejected. However, if the designer could make the product more tolerant to $V_{DD}$ and/or $T$ variations, more reliable devices could be delivered, higher yield would boost profitability and operation-dependent “faults” would not trigger erroneous behaviour, increasing dependability. Recently, a VT-aware (power supply Voltage and Temperature) design methodology has been proposed [2][3], which aims at increasing tolerance to VT variations, even in the presence of process variations, without compromising circuit performance and testability. The methodology, which uses the concept of dynamic time borrowing, was demonstrated with variable (but ideal) voltage sources, $V_{DD}$, and for digital circuits in normal operation modes.

In order to detect physical defects in emerging nanometer semiconductor technologies, delay test is required, which incorporates static and dynamic test [3]. By using delay test to identify circuit defects, Boolean values and timing responses must be compared to their fault-free counterparts. For this propose and especially if lifetime self-test is part of product specification, dynamic BIST (Built-In Self Test) is required, as well as scan.

1.1. Context and Objectives

The general objective of the work reported in this Dissertation is to develop a design and test methodology to increase tolerance to VT variations (namely, due to PSN and power consumption), while keeping the ability to ensure high delay fault coverage.

The framework to achieve this goal is the VT-aware design methodology under development in the Quality, Test and Hw/Sw co-design R&D Group at INESC-ID, namely in the DynaTest FCT project. However, several questions need an adequate answer:

- Does the proposed methodology hold its tolerance gains, and its ability to uncover delay faults in a multi-$V_{DD}$ test environment, when non-ideal power supply voltages are used, inducing a significant power noise?
- Is the conclusion valid, not only for classic non-ideality of $V_{DD}$ (IR voltage drop, in power resistive layers), but also when inductive effects become relevant (namely in high frequency operation)?
- Can the proposed VT-aware methodology be used in logic circuits, generated with a DfT (Design for Testability) technique, like BIST or scan?
- Is the dynamic time borrowing concept useful both in normal and test modes of operation?

The specific objective of this Dissertation is to provide answers for the above questions, developing a methodology to carry out performance evaluation, using circuit level simulation, providing evidence to the answers, and design guidelines to increase the effectiveness in using the VT-aware methodology.
1.2. Methodology

As referred, the objective of the work is to analyze the effectiveness (and limitations) of the VT-aware methodology in the presence of non-ideal power supply voltages and in a DfT environment, using BIST or scan design techniques.

Real world power supply sources deliver to IC cores noisy supply voltages, even for a single power domain (a subset of the chip power grid). In fact, the real $V_{DD}$ voltage source must be represented as a distributed RLC network, driven by a non-ideal voltage source.

Using combinational, pipeline and FSM (Finite State Machines) digital circuits, in a multi-$V_{DD}$ environment eventually using scan or BIST structures, one must find out, when the VT-aware methodology is used in the design flow, (1) if the tolerance gains to VT variations hold, (2) if fault detection is kept, and (3) if the discrimination between fault-free and defective parts is performed due to timing errors occurring only in the CUT (Circuit Under Test), in normal or test mode, or in the test circuitry, or in both. We do not want to have false positives or false negatives, due to errors occurring in the test circuitry.

The purpose of this Dissertation is to set up a method to investigate these issues, and answer to the above questions. An EDA environment, with commercial tools (Cadence, Synopsys) and an INESC-ID proprietary tool, DyDA (Dynamic Delay Analyzer), is used. A target IC CMOS technology is selected. A simulation set-up is devised, especially for circuit-level simulation under variable $V_{DD}$ and/or $T$. A set-up circuit is proposed, to emulate variable circuit complexity and power supply voltage non-ideality. Test stimuli are defined. A set of test vehicles (industrial and benchmark circuits) is used as demonstrators. The parametric search space is defined, to broaden the validity of the conclusions. The impact of $V_{DD}$ non-ideality is studied, first due to resistive IR drop, then due to IR drop and inductive effects. Test vehicles are simulated in a BIST or scan environment, and circuit behavior and performance, in normal and test modes, is analyzed. Different implementations of the VT-aware methodology are also experimented. Finally, delay fault detection of resistive bridging defects is performed, in a multi-$V_{DD}$ test scenario. Results under variable temperature are also computed.

1.3. Relevant Contributions

The most relevant contributions of this work are as follows:

- To devise a methodology to experiment the VT-aware design methodology under non-ideal power supply voltage sources, in digital circuits with DfT;
- To propose a set-up lumped circuit, with two model parameters (the gain factor, $G$, and the unit resistance of the metal power supply lines, $R$), to emulate digital circuit complexity, and local power grid non-ideality;
- To thoroughly analyze digital circuit timing response in presence of power supply noise (PSN);
- To demonstrate, by simulation, that the VT-aware design methodology holds in the presence of PSN, for circuits with test circuitry associated to the use of DfT techniques, like BIST and scan;
• To demonstrate that the dynamic time borrowing concept, associated to the insertion of VT sensors and delay actuators, referred as DDB (Dynamic Delay Buffers) cells, can be applied in DfT circuits, in normal and test mode, leading to enhanced tolerance to VT variations, while still allowing delay fault detection in a multi-$V_{DD}$ test (or self-test) environment;

• To demonstrate that the proprietary software tool, DyDA, is effective in identifying (with PrimeTime™) circuit critical paths, defining maximum frequency of operation and proposing the number and location of DDB cells to be inserted, either in the clock signal path of some registers, or in the signal path of some short delay paths in the data path.

1.4. Document Outline

The Dissertation is organized as follows. In chapter 1, a brief introduction in which the context of the work is presented, the relevance of the addressed problem is highlighted, and the methodology followed to carry out the work is presented. In chapter 2, a survey of the related work is presented. In chapter 3, the proposed methodology is described, including the EDA environment, simulation set-up, case studies and search space. Chapter 4 characterizes the impact of the non-ideal power supply voltage on timing behavior. In chapter 5, a sequential benchmark circuit, B06, is used with scan, to show the improvements (in normal and test modes of operation) on tolerance to $V_{DD}$ variations, in a multi-$V_{DD}$ test environment. Chapter 6 presents the simulation results for several industrial circuits, in a BIST and pipeline environment, exploiting the parametric search space, and demonstrating the effectiveness of the methodology for delay fault detection. Finally, in chapter 7 the conclusions and directions for future work are presented.
2. State of the Art

Temperature and power supply voltage are two crucial parameters that have to be taken into account when circuit performance is defined, according to circuit specifications. High performance systems lead to high power consumption, which must be constrained. Hence, many low-power design techniques have been proposed [4][6]. One relevant problem is power consumption in test-mode, which typically exceeds power in normal mode of operation, due to the need of higher switching activity. Anyway, overheating can occur during SoC testing. Hence, architectural solutions and test scheduling algorithms have been proposed in order to handle the problem [7]. Hot spots (including temperature gradients), global warming (due to SoC operation) and physical adjacency of multiple cores are the main causes for performance variations of a local module or IP (Intellectual Property) core, which modify the dynamic behavior of the CUT.

Power saving design techniques can take advantage of power supply voltage ($V_{DD}$) reduction and consequent energy decrease. These factors are crucial for portable equipment applications. A rewarding design technique, DVS (Dynamic Voltage Scaling), has been proposed [7], and has been under intense research [8][9]. This technique is now used in commercial products, e.g., ARM (IEM) [11], AMD (PowerNow) [12], INTEL (Xscale) [13] and TRANSMETA [14]. Processors that incorporate DVS typically have, on-chip, an operating power supply voltage range from full to half of nominal $V_{DD}$ [8]. Scaling $V_{DD}$ can also allow clock speed reduction (under performance specifications compliance), which additionally decreases power consumption. In fact, DVS is frequently used as a DVFS (Dynamic Voltage and Frequency Scaling) technique to further enhance power and energy reduction.

The availability of variable power supply voltage on-chip can also be exploited for test and diagnosis purposes, in the context of multi-$V_{DD}$ schemes [15] in BIST solutions for delay testing [16].

The DVS-based multi-$V_{DD}$ test in a BIST environment can efficiently be used not only to detect delay faults, but also to diagnose them. A multi-$V_{DD}$ based self-test scheme is proposed in [17], and its usefulness is demonstrated for resistive open and bridging defects.

In this context, this dissertation exploits $V_{DD}$ variation, in order (1) to derive design solutions with enhanced tolerance to VT variations, under severe power supply noise (PSN) effects, (2) to check that delay fault detection is still possible, when the VT-aware design methodology is used, although requiring lower $V_{DD}$ values in the multi-$V_{DD}$ test environment.

2.1. Semiconductor and Test Technologies

Technology is a very important constraint that must be taken into account in the design process. IC technology is being pushed down to its physical limits. Many emerging problems start to appear, in technologies bellow 40 nm, namely on novel die defect mechanisms and process variations. The susceptibility to PSN and temperature variations is increasing.

Defect and fault modeling are crucial issues in DfT (Design for Testability). In fact, as new defect mechanisms emerge, new defects and faults must be identified, modeled and diagnosed, for fast yield ramp-up.
2.1.1 Physical Defects

A defect is described as a physical imperfection on the manufactured chip, due to substrate inhomogeneities, or induced during wafer processing.

There are several defect types in packaged chips, which may be classified as processing defects, material defects, time-dependent failures and packaging failures [18].

Processing defects are produced by extra or missing conductive material, parasitic transistors or oxide breakdown such as thin oxide pinholes. Material defects may have their source on bulk defects, such as cracks or crystal imperfections, or in surface impurities like ion migration. Time-dependent failures are induced by dielectric breakdown or electromigration. Finally, packaging failures may be produced by contact degradation or seal leaks.

Defects can be categorized in critical and non-critical defects as showed in Figure 1. A non-critical defect is a defect that does not cause the circuit to fail; hence, its occurrence can be tolerated, as it doesn’t interfere on die profitability\(^1\). Critical defects cause a single or multiple bridging (BRI) fault, depending on the number of adjacent tracks that are affected.

One of the difficulties associated with uncovering defects are the large number of possible defect classes, e.g., open vias, floating gates or material shorts. Non-equiprobable failure mechanisms can span in magnitude orders the likelihood of occurrence of individual faults. Technology dependent defect classes are another issue, as technology is always changing and improving. Hence, new defect classes are being identified and characterized. For test preparation, a realistic fault list may lead to a computational problem, due to the huge number of possible defect locations, for each defect class.

2.1.2 Faults and Fault Models

A fault is usually an abstract representation of a physical defect. It models, at a given level of abstraction, the impact of a physical defect on circuit behavior. Such impact is not visible at the circuit’s output response to all input vectors. Usually, only a limited subset of input vectors of the input space lead to output responses that differ from the correct response. These input vectors, when applied to the circuit, allow uncovering the likely faults, i.e., allow fault detection. In order to guide the test generation process, Fault Models (FM) has been developed to describe the likely physical defects [7][16][20].

\(^1\) Non-critical defects may cause reliability problems, as device operation may, along product lifetime, cause infant mortality.
Fault Model leads to the generation of test patterns with few input vectors, i.e., lead to short test length (TL). These are referred as deterministic test patterns. In order to achieve an accurate representation of the defect behavior, FM must present some characteristics, such as (1) to present at least a gate-level of abstraction, a Boolean behavior of the defective device, (2) to lead to a fault list as short as possible and (3) to allow TPG in such a way that each single vector may detect a significant number of faults.

Depending on the abstraction level (register transfer, gate, transistor level), fault models may be classified. Hence, they can be static or dynamic, arbitrary or realistic. Some arbitrary fault models are the single Line-Stuck-At (LSA), multiple LSA, transistor stuck-open and transistor stuck-on. Realistic fault models are bridging nodes, open multi-layer physical nodes, memory faults, PLA (programmable logic array) faults and delay faults.

In this work we focus our attention on fault models described at logic or electric level, like resistive BRI or open faults.

2.1.2.1 Line Stuck-At Faults
The Line Stuck-at faults are modeled by assigning a fixed logic value, 0 or 1, to a signal line of the circuit, an input or output of a logic gate or a flip-flop [16]. The impact of any defect occurring in given device or at given interconnection is assumed to produce a single erroneous (complementary) logic value at a given line of the circuit.

Depending on the fixed value the fault could be single line stuck-at 0 or single line stuck at 1. This fault model assumes that a single fault can exist in the circuit at a given time.

In order to detect a stuck-at fault a test vectors is needed. The TPG tool generates a partially specified test vector that activates and propagates the fault to an observable output. Test vectors are usually generated by an Automatic Test Pattern Generator (ATPG) tool. Deterministic TPG leads to low test length.

2.1.2.2 Bridging Faults
A bridging fault represents a short between a set of signals [21]. At gate level, the short can become a 1-dominant (OR bridge), 0-dominant (AND bridge), or indeterminate depending upon the implemented technology.

Bridging faults are distributed between two basic types, feedback and non-feedback bridging. If it exists in the circuit at least one path between two lines, then a bridging effect between those lines creates one or more feedback loops. Feedback bridging fault may transform a fault-free combinational circuit into a faulty sequential circuit. The fault coverage of test patterns generated for LSA fault detection may not lead to 100% bridging fault coverage, in the presence of feedback bridging faults. Non-feedback bridging faults are combinational and the fault coverage by LSA test vectors is normally very high.

2.1.2.3 Delay Faults
A Delay Fault causes the signal propagation delay of a circuit to exceed the clock period, which may lead to a timing fault. There are different delay fault models, such as transition faults, gate-delay faults, line-delay faults, segment-delay faults and path delay faults. The two more relevant delay fault models are the transition faults and the path delay faults.
Transition faults are the type of faults that make the signal change on a line be slower than the normal value. There are two types of transition faults, slow-to-rise and slow-to-fall. In order to detect a slow-to-rise fault, a LSA0 test is applied. This test will set the line value to 1 in the fault-free circuit and propagate the state of the line to a primary output, so if the line is slow-to-rise the produced result is 0 at the output instead of 1.

The advantages of this fault model are the limited number of faults (twice the number of lines). Tests are easy to generate and circuits that present high stuck-at fault coverage usually also covers transition faults [16]. These faults have been used in industry and it is recommended that they be augmented by some path delay tests, at least for the critical paths.

Path Delay faults occur when the cumulative propagation delay of a combinational path increases over an upper bound (clock period or vector period). For each combinational path, there are two path delay faults, the rising and the falling clock transitions. The analyzed path begins at a primary input (or clocked flip-flop) and ends at a primary output (or clocked flip-flop). The time to propagate a logic switching through the path is the propagation delay. The path length is defined by the number and nature of logic gates in the path.

This fault model is usually used to detect small delays in the path, that are not detected by the transition fault model, as the extra delay in each gate is very low.

In general, the number of circuit paths is very high, and increases exponentially with circuit complexity, which may render TPG costs prohibitive. Moreover, it is difficult to identify when exactly a test fails, which leads to the use of statistical processes and accurate simulations [19].

2.1.3 Built-In Self Test (BIST)

External test is not always the most cost-effective solution. Hence, BIST (Built-In-Self-Test) can become an attractive solution [31]. Figure 2 shows the block diagram of a typical BIST structure, where the TPG is implemented by a Linear Shift Register (LFSR). The TAE (Test Answer Evaluator) is implemented with a Multiple Input Shift Register (MISR). The test process is controlled with the “BIST controller” [4]. The MUX selects data from the PI (Primary Inputs), or from the LFSR.

In normal mode, PI drives the CUT inputs, and the CUT PO (Primary Outputs) are observable. In test mode, the BIST controller receives a BIST start signal, and generates a signal to the MUX in order to select the inputs produced by the LFSR. The CUT response is captured by the MISR. At the end of the BIST session (n clock cycles), the signature is captured in the MISR, compared with the circuit correct signature, and the comparison result is reported (Pass/Fail). The BIST controller determines if the results are valid by putting to the output the high stage at BIST done [16].
2.1.4 Scan Design

Scan design is a structural method of DfT for digital circuits. The goal of this method is to control and observe the internal flip-flops, by adding a test mode. When the circuit is in test mode, the flip-flops are reconfigured into one or more shift registers. The inputs and outputs of these shift registers are made into primary inputs and primary outputs. The block diagram is presented on Figure 3.

2.1.5 Process, Voltage and Temperature (PVT) Variations

Process variations are becoming an authentic master mind for test engineering, once technology is constantly in evolution, which leads to a demand of increasing performance and reduced size. Increased power density and temperature have a significant impact on circuit performance, power consumption, reliability and cooling and packaging costs, which leads to a thermal-aware design issue.

Process, power supply voltage and temperature variations may lead to signal integrity problems, i.e., may lead to problems in the ability to generate correct responses in a circuit. For System-on-Chip (SoC), several signal integrity problems have been under research, in particular overshoot/undershoot, power supply noise (PSN) and signal skew [20].

The overshoot or undershoot problem is defined as the transient signal rise / decrease above /below the $V_{DD}$ value and $V_{SS}$ value. PSN is internally generated and the noise value is proportional to the signal swing. Noise in power and ground rails influences the signal levels.
Signal skew is another problem related to process variations. If the arrival time of a signal suffers a delay, it will arrive at different instants to the output, which may lead to the capture of an erroneous value.

Power supply and temperature disturbances have a huge impact on circuit performance, as they modulate the propagation delay through signal paths.

In order to outline the power dissipation from the over-heating of the circuit and to eliminate costs a new approach was developed in [23]. Power consumption is directly connected to the energy costs. Power density is increasing because of the technology evolution. Adequate thermal solutions are very difficult to apply to the new circuits. Hence, novel techniques, known as Dynamic Thermal Management, have been proposed [24].

Improving tolerance to power supply and temperature variations is a goal that is technology dependent, which means that is always being updated.

### 2.2. Low Power (LP) Design

Low power design techniques are mandatory for successful product development. Chips for portable electrical devices are required to reduce the power, in order to increase batteries life, which leads to new constraints. IC technology is a moving target. Clock frequency is ever increasing. Reducing power dissipation is a serious issue. In static CMOS, power dissipation is proportional to $V_{DD}^2$. With the power supply voltage, $V_{DD}$, being lowered, also MOS transistors threshold voltages have to decrease, which increases leakage power, as sub-threshold leakage increases exponentially with gate-source voltages. For instance, when new 65nm and 40nm IC technologies are used, dynamic power $^2$ and leakage power $^3$ may be similar. Hence, LP techniques often strive to restrict leakage power.

In order to create low power designs, new tradeoffs must be taken into account at different stages (and different levels of abstraction) of the design flow [25]. Tradeoffs can be timing versus power or area versus power, depending on the design stage.

Several techniques have been developed, like clock gating, multi $V_{th}$ (MOS transistor threshold voltage) libraries, power gating, voltage islands, clock power optimization, dynamic voltage scaling (DVS), dynamic frequency scaling (DFS), among others.

#### 2.2.1 Power Domains

In high-performance low power design, not all functional modules require the same amount of time for data processing. Hence, to save power, power supply voltages, feeding each module, should be as low as possible, without violating the performance specifications. Moreover, as referred, unwanted $V_{DD}$ variations (operation-dependent) are a main source for performance degradation. Power consumption also induces thermal variations, including temperature gradients along the die, which can further degrade circuit performance. In order to decrease PSN, and to provide different $V_{DD}$ values for different modules, the overall chip power grid is partitioned in sub-grids, often using different output ($V_{DD}$ and $V_{SS}$) pins. Each sub-grid constitutes a power domain.

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$^2$ Dynamic power is the power a device consumes when a user is employing it for intended purpose.

$^3$ Leakage power is the power wasted by leakage transistors.
In each power domain, designers need to estimate circuit power consumption, especially in the test mode, as the power consumption is different, depending on the operation mode [25]. There are many reasons for a digital circuit, operating in a test mode, to consume more power. Test planning may schedule the test of multiple modules in parallel. The clock frequency at which tests are performed directly impacts power consumption (dynamic tests need to be performed at-speed). Enhanced switching activity also increases higher power consumption. DfT techniques, like scan design, may also be responsible for added test power: for instant, research is under way to restrict power consumption during the shift-in and shift-out operations. In test mode, power consumption is typically constrained (as a design specification) not to exceed twice the power consumed in the functional.

Test power consumption may play an active part in device reliability, system design, and in other aspects of the physical design, such as power grid design and packaging.

Many solutions have been proposed to restrict power consumption in each power domain design, like Power Gating, Power Switches, Data Retention and Voltage Islands.

Power Gating is a technique that involves the temporarily shutting down of design modules that are not being used. This is a complex technique that implies a design of a power controller which identifies the blocks that must be shut down and the moment for that to happen, as well as the voltage that should be applied to different blocks. Normally there are two power gating methods, the fine-grained and the coarse-grained. In the fine-grained, a switch transistor between ground and each gate is used. The benefit is that this technique leads to a fairly easy power characterization of each cell. The drawback is area overhead. The coarse-grained is the alternative approach that uses a power switch network, a group of transistors that in parallel turn entire blocks on and off. This technique is very hard to characterize in a cell-by-cell basis.

Power Switches are used to gate the power supply connection to $V_{DD}$ and/or GND. Usually they are implemented with high-$V_{th}$ PMOS (NMOS) transistors. By introducing this technique, it is possible to turn on or off the power supply voltage source available to the core. In order to avoid current surges due to simultaneous switching, power switches are typically connected in daisy chains. The power switches test need to be taken into account, as the presence of a defective switch in multiple power switches can mask test results.

Data Retention aims at preserving the state of memory elements in a circuit when the Power Switch technique is used and modules are shut down. When a core is power gated by a transistor that controls core’s power supply voltage, this core can be wake-up or shutdown. If the core is going to be shutdown it is important to maintain its state, in order to prevent the information lost. This way when the core wakes-up it presents the correct stage. This technique implies an area overhead, as it requires an extra memory cell to maintain the state. This new memory cell can not be power switched, in order to preserve information.

Voltage Islands is a technique used when multiple power domains are designed, requiring interface circuitry. By implementing this technique with on-chip switches, floor planning becomes more complex.

2.2.2 Clock Domains

Power variations can make signals to arrive too late or too soon at key nodes of the circuit. Such timing-faults, not due to a physical defect, are operation-dependent.

In LP design, the operating frequency is a major constraint in the circuit behaviour. Among panoply of techniques, it is worthwhile to mention clock gating and dynamic frequency scaling. Moreover, time borrowing
techniques may modulate clock skews. In particular, the VT-aware methodology described below uses Dynamic Delay Buffers to locally modify clock phase.

Clock Gating is probably the oldest technique for reducing power. The basic concept is: if there the design don’t need a clock running at that time, then the clock is shut down. Both local and global clock gating can be used. In local clock gating, multiplexers are identified. If there is a feedback multiplexer, it is replaced by a clock-gating cell that clocks the signal off. With this technique significant power savings can be obtained. Global clock gating turns off the clock of whole block; typically, this is done using a central-clock-generator module.

Dynamic Frequency Scaling is a design technique, commonly used in mobile systems, in which the operation frequency is defined, if possible, to be less-than-maximum frequency.

Dynamic Delay Buffer (DDB) is a cell developed using the Time Borrowing (TB) principle. It operates as a Voltage-Temperature sensor, and acts by inserting a variable delay $\tau(V_{DD}, T)$ [27]. The typical DDB cell is composed by two unbalanced inverters with slow PMOS transistors and two additional balanced inverters to restore fast transitions at DDB output [3] (Figure 4). We refer this configuration as architecture $a_2$. The core of this cell is the two unbalanced inverters (referred as architecture $a_1$).

Area and power overhead can be minimized by designing TB flip-flops, this way the DDB cell would be part of a flip-flop. The proposed methodology adapts the clock delay (skew) locally and dynamically, depending on VT variations, thus avoiding erroneous logic values to be captured and processed.

Figure 4- Architecture of a DDB cell (architecture $a_2$).

2.2.3 Variable $V_{DD}$

Unwanted $V_{DD}$ variations are introduced by power supply noise (PSN). $V_{DD}$ variations, namely voltage drop effects, are very important as signal propagation times are modified. This can make the circuit to fail timing specifications.

Power supply voltage variations are becoming more relevant, as the resistivity of the power and ground tracks is not negligible. These effects can be reduced (but not solved) by increasing the width of power and ground tracks.

$V_{DD}$ variations can be determined by design. A design technique that presents voltage variation is the Dynamic Voltage Scaling (DVS). This is an aggressive technique used for power management in advanced microprocessors. In this technique, variable $V_{DD}$ is applied as required to minimize power consumption, while keeping circuit performance. In principle, both over-voltage and under-voltage can be applied.

In this dissertation $V_{DD}$ variations are extensively investigated, both in unwanted (PSN) and wanted (delay fault detection) contexts.
2.3. Low Power Testing

With device scaling down, the test process of LP circuits is becoming more challenging. As result, Design-for-Testability (DfT) techniques need to be developed, including test generation and application processes.

With low power devices being implemented on deep submicron technologies, power management becomes a critical constraint that cannot be ignored. In order to evaluate the power consumption of a system under test, three parameters have to be taken into account, namely consumed energy, average power and peak power.

The consumed energy is mainly due to the energy required by the switching activity occurring in the circuit during test application.

The average power consumption is computed by the ratio between the energy and the test time. Hot spots and reliability problems may have their source on power consumption. One of the reasons for considering this parameter during test is that test power exceeds the power consumption in normal mode.

The peak power consumption is observable by the switching activity in the circuit for specific clock cycles, where many logic gates and registers switch their logic values. It is a useful parameter for the evaluation of thermal and electrical limits, as well as system packaging requirements.

There are two categories of power consumption in CMOS circuits, static and dynamic. The first one has its origin basically on leakage current or other current drawn continuously from the power supply. The second one is basically due to the charging and discharging of load capacitances during logic switching [28].

As referred, many problems occur due to excessive test power consumption. Practical, industrial solutions include over sizing power supply, package and cooling in order to stop the current increase during test (avoiding hot spots); reduction of operation frequency during test and the partitioning and test planning of the test circuit.

Avoiding hot spots by current control is a solution that brings a hardware increase and test application time, which represents a cost increase. Reducing the operation frequency is a problematic solution, as it increases test application time and may lead to fault masking of dynamic faults, with a consequent reduction on defect coverage. Test partitioning and planning allows the detection of dynamic faults, at a cost (test overhead).

Another constraint that must be taken into account is cost limitations. For consumer electronic products, low cost makes the use of plastic packages mandatory. However, this limits power dissipation. This may force the use of special packages, or cooling systems, to keep the thermal conditions under the specifications, which may again trigger cost increase.

2.3.1 Delay Testing

Delay test is required to verify correct at-speed circuit operation. Delay test may be applied as a functional test, or as a structural test. Functional test is carried out by Speed Binning. Structural test incorporates the Path Delay Test and the Transition Delay Test. When sensitivity to PVT variations is under scrutiny, structural delay test is crucial, and is briefly described in this section.

The three most common approaches to transition delay test, associated with deterministic at-speed test are Enhanced Scan, Launch on Capture (LOC) and Launch on Shift (LOS) [4]. In Path Delay Test, it is assumed
that the presence of a delay fault (described in section 2.1.2.3) increases the signal propagation delay along the path. The advantage of path delay test, as compared to transition delay test, is the fact that it can represent gate and interconnects distributed delays in the circuit, which may be affected by device parameter variation and by single isolated failures. A disadvantage is the test overhead, i.e., the extra hardware required to implement this test technique, which increases chip area and may cause a degradation of circuit performance. However, single fault assumption may no longer be realistic since a single defect affects a large number of paths. With path delay test robust and non-robust test need to be considered [32]. A robust test detects a delay fault in spite of all other delays and delay faults in the circuit. A non-robust test detects a fault with the assumption that no other delay fault exist in the circuit.

The paths considered in path delay test are the critical paths. Timing analysis examines the circuit combinational paths, taking into account gate and interconnection delays. The timing analysis results are used to improve circuit design and testability and can be performed through timing simulation, critical paths test or layout optimization. However, it may not always guarantee 0 DPM (Defective Parts per Million) production test.

2.4. VT Aware Design Methodology

The problem to be solved is to increase circuit tolerance to VT variations, even in the presence of process variations, without performance or testability degradation.

In the proposed VT-aware design methodology, which is the core of Jorge Semião’s Ph.D. thesis [27], a dynamic time borrowing strategy is used to delay the clock signal driving specific memory cells, providing additional time to accommodate the increased signal propagation delay through the logic whose VDD or temperature is being disturbed. We refer these registers as CME (Critical Memory Elements). This allows controlling the instant of the active clock edge trigger for the memory cells with the smallest time slack margin.

Dynamic time borrowing is implemented by modulating the clock phase of pre-determined CME [3][33]. VT variations sensing and on-line delay insertion in the clock signal path driving CME is performed through Dynamic Delay Buffer (DDB) cells [3]. First, the underlying principle of the methodology is explained.

The principle is illustrated in Figure 5. When a VDD reduction (or T increase) occurs, typically the propagation delays in signal paths increase. This may lead to synchronization errors in memory cells driven by the circuit critical paths (CP). The solution is to dynamically adapt the clock skew of the CME, in order to allow them to capture the correct data. This is accomplished, by adding a DDB cell to each CME. A DDB is, thus, a minimum overhead cell placed in the clock signal path of a CME. Time is borrowed [34] from the subsequent pipeline stages to accommodate the delayed signal, while maintaining at-speed clock rate. A simple architecture for the DDB cell (here referred as architecture a1) is shown in Figure 6, using two unbalanced inverters, with slow PMOS transistors [3]. This architecture is used when the input stage of the storage element (the CME) has a buffer in the clock line. The DDB cell
inserts a variable delay $\tau(V_{DD}, T)$. The required amount of delay, and of delay variation with $V_{DD}$ or $T$, for correct operation, depends on the critical path’s propagation time. The longer it takes signals to propagate through the critical paths, the longer should be the delay, $\tau(V_{DD}, T)$, inserted by the DDB cell. An analytical model is used to design the aspect ratios of the 4 MOS transistors [3]. A second architecture is proposed in [33], using two additional balanced inverters (architecture $a_2$), to restore fast transitions at DDB output. This DDB implementation is depicted in Figure 5 and used throughout this work. Sizing appropriately the transistors allows changing the DDB delay value and dependence on VT variations. Area and power overhead introduced by the DDB cells can be minimized, by designing TB Flip-flops (time borrowing FF), integrating the DBB in the conventional FF [34].

![Figure 5-Underlying principle of the VT-aware time management methodology.](image1)

![Figure 6-Schematics of a possible implementation of the Dynamic Delay Buffer (DDB) cell (architecture $a_1$).](image2)

The innovative idea in the proposed methodology is to adapt the clock delay (skew) locally and dynamically, as needed. Clock delay may be temporarily modified for some functional parts of a SoC, but maintained unchanged for the other parts. This does not result in a circuit functional error if all the combinational parts of the circuit keep on working synchronously. The proposed methodology is an error avoidance technique, which is better than error detection and correction in a subsequent clock cycle, like the RAZOR technique [29][30]. RAZOR uses a shadow latch which is controlled by a delayed clock.

The amount of tolerance to VT variations gained with the implementation depends on the assumed VT variation domain, and also on the target digital module. The amount of dynamic delay insertion using DDB cells is a design parameter. However, the more time you borrow in a combinational stage, the more time you must recover.

Using the above underlying principle, two consequences need to be considered. First, for correct operation, time management [27] must be carried out in such a way that the borrowed time must be recovered in a subsequent stage. Second, when a given $\Delta \tau$ interval is borrowed in stage $i$, output $j$, the correspondent signal $Q_j$ is delivered by the CME to the correspondent input of the $(i+1)$ stage with a $\Delta \tau$ delay, which modifies the
propagation delay times of the \((i+1)\) stage. These two consequences introduce limitations to the correct circuit operation, namely in digital circuits with short delay paths, in pipeline and in sequential circuits\(^4\) [27]. Such limitations may require DDB insertion in short delay signal paths (without degrading circuit performance).

### 2.4.1 Critical Path and \(f_{\text{max}}\) Identification

In order to implement the proposed methodology, the designer needs to identify the critical paths (CP) and the maximum frequency of operation, \(f_{\text{max}}\), taking into account a domain of assumed parametric variations. Typically, worst-case designs consider a temperature range (commercial, or military specs), a \(V_{\text{DD}}\) range \((V_{\text{DD}} \in (0.9, 1.0) \ V_{\text{DDnom}})\) and a range of technology-dependent process variations. Due to these parametric variations, not only the longest signal path is identified (\(\tau_o\) delay), but also all CP that lie, for nominal conditions, within a typical range of \(\alpha \tau_o\) \((0.9; 1.0)\). Worst-case design leads to large performance degradation, due to the need to introduce a safe time slack margin.

CP and \(f_{\text{max}}\) evaluation can be carried out at different abstraction levels. The lower the abstraction level, the more accurate the evaluation is performed. In the VT aware methodology, CP and \(f_{\text{max}}\) computation is carried out at logic level, using Static Timing Analysis (STA) (with Synopsys PrimeTime™ tool). At logic-level, the maximum frequency of operation is estimated, for nominal conditions, as \(f_{\text{max}} = 1/\tau_o\). Circuit-level simulation can latter be used to refine the \(f_{\text{max}}\) values, for the identified CP. In this work, CP are identified at gate-level, and \(f_{\text{max}}\) is computed directly at circuit-level. In order to compute \(f_{\text{max}}\), a Cadence script was developed. Circuit simulation is first performed at low frequency, which allows the computation of the circuit correct signature (e.g., compressed by a MISR). This value is recorded, and an additional circuit simulation is carried out, doubling the frequency. If a correct signature is obtained, the procedure is repeated, until an erroneous signature occurs. When this happens, additional simulations are performed, now lowering the last clock frequency, until a correct signature is again obtained. The frequency for which this is achieved is \(f_{\text{max}}\).

### 2.4.2 DDB Insertion Criteria

A key process of the methodology implementation is CME selection. An INESC-ID proprietary tool, *DyDA*, which stands for Dynamic Delay Analyzer, is used to perform dynamic delay insertion, in order to automatically perform CME selection and DDB insertion analysis [27]. This analysis is based on the calculation of the expected time slack margins improvements achieved with each DDB insertion. The purpose of each CME selection is to enhance the time slack margin of the critical path. DDB insertion is first performed in the most critical memory cell, time slack margins are up-dated, and the procedure is repeated until no more improvements can be obtained. After DDB insertion, static timing analysis (STA) may uncover the need to insert a DDB cell in a short delay path. For each design, more than one level of tolerance improvements can be defined, depending on the number of DDB

\(^4\) For instance, if the design of a FSM has a critical path in a feedback loop, the methodology cannot be applied.
to be inserted. Single or multiple DDB insertion can be carried out (1) in the clock path, for each assigned CME, and (2) in the signal path, for each short data path that requires it. The best location for DDB insertion in short delay paths is also considered. The designer selects the final solution, after trade-off analysis.
3. Proposed Methodology

The methodology proposed in this dissertation is implemented and demonstrated using an EDA (Electronic Design Automation) environment, and a target CMOS technology.

3.1. EDA Environment and Target CMOS Technology

3.1.1 Cadence

In the semiconductor industry, Cadence™ is one of the most widely used EDA vendor delivering a powerful environment and set of software tools to perform low power design, verification and implementation of electronic systems [35]. In this work the technology platform used was “Virtuoso custom IC design”. Electrical simulations were performed with “Virtuoso Spectre Circuit Simulator” that provides fast and accurate Spice-level simulation for analog and mixed-signal circuits.

The EDA environment was used with CMOS static digital circuits, implemented with “Cadence AMS Methodology Kit” using 0.35 μm CMOS technology design kit (c35b4). Although more aggressive IC technologies should be used, the available technology with detailed electric-level information (even for Monte Carlo simulations) was the Austria Micro Systems™ (AMS) 350 nm CMOS technology. Hence, this IC technology was used throughout the work.

3.1.2 Synopsys

In order to complement the simulation environment provided by Cadence, Synopsys™ synthesis and simulation tools are essential in the design flow. Synopsys suite presents a huge number of solutions in multiple domains, such as low power design, design platforms, verification platforms or design for manufacturing [36].

In this work, two Synopsys tools, namely “Design Vision” and “Primetime”, were used. The first tool was used for circuit synthesis and simulation, including performance analysis. The second one was used for static timing analysis (STA), especially for time slack analysis. Time slack may be defined as the time interval difference between the clock period and the time interval associated with the time response of the critical path in the slowest combinational module between registers.

3.1.3 Proprietary DyDA Tool

The tool starts with the VERILOG RTL description of the digital system. The first process is to perform STA, identifying circuit critical paths and short paths. For this, DyDA instantiates a commercial EDA tool (as referred, Primetime™, from Synopsys™).

A key process of the VT-aware methodology implementation is CME selection. DyDA automatically performs CME selection and DDB insertion analysis. This analysis is based on the calculation of the expected time slack margins improvements achieved with each
DDB insertion. The purpose of each CME selection is to enhance the time slack margin of the critical path. The algorithm tests DDB insertion in the most critical memory cell, updates the time slack margins, and repeats the calculus until no more improvements can be achieved or when a violation occurs (like feedback loops in CME). After DDB insertion, STA may uncover the need to insert a DDB cell in a short delay path. For each design, more than one level of tolerance improvements can be defined, depending on the number of DDB to be inserted. When the designer selects the final solution, the VERILOG code is modified, by adding predefined DDB cells.

### 3.2. Multi-frequency and Multi-V\textsubscript{DD} Test

Three parameters influence system’s operation and performance, and can be used to enhance the panoply of external or built-in dynamic test techniques: clock frequency (\(f_{\text{max}}\)), power supply voltage (\(V_{\text{DD}}\)) and temperature (\(T\)). However, the impact of these three parameters on a digital module, IP core or SoC performance needs to be computed, in the design environment, in order to develop new test and DfT techniques.

Supply voltage and temperature variations may occur, either intentionally (especially \(V_{\text{DD}}\) variations) for design, test and diagnosis purposes, or unintentionally as part of system operation. In both cases, their impact on system performance must be accounted for.

Power consumption and power management are critical design problems, and many low-power design techniques have been proposed [37]. However, power consumption in test mode is also a relevant problem. Hence, overheating can occur during SoC testing. Architectural solutions and test scheduling algorithms have been proposed to tackle this problem [28][38].

Global warming (due to SoC operation) and hot spots (inducing temperature gradients) cause performance variations (in time and space) of a local module or IP core, which modifies the dynamic behavior of the CUT (Core Under Test). Physical adjacency of simultaneously active cores can also induce T gradients and timing distortions. CUT operation can also cause variations on the assumed static \(V_{\text{DD}}\) value, due e.g. to EMI, ESD or power noise.

Power saving design techniques can take advantage of \(V_{\text{DD}}\) reduction, leading also to energy reduction, crucial for portable equipment applications. A rewarding design technique, DVS (Dynamic Voltage Scaling), has been proposed [7][8]. Several power management techniques have been recently proposed, and some have migrated to industrial products, e.g., ARM (IEM) [11], AMD (PowerNow) [12], INTEL (Xscale) [13] and TRANSMETA [14]. Current processors that incorporate DVS typically have, on-chip, an operating power supply voltage source delivering variable \(V_{\text{DD}}\), ranging from full to half of nominal \(V_{\text{DD}}\) [8]. Scaling \(V_{\text{DD}}\) also allows to reduce clock speed (under performance specs compliance), which additionally decreases power and energy consumption. In fact, DVS is frequently used as a DVFS (Dynamic Voltage and Frequency Scaling) technique.

The availability, on-chip, of variable power supply voltage can also be exploited for test purposes, namely for multi-\(V_{\text{DD}}\) test schemes [9] in scan or BIST solutions.
For several IC technologies (namely, for 0.35 μm and 130 nm CMOS technologies), it was shown [17] that an identical impact on timing response can be emulated by ΔVDD or by ΔT. Moreover, the effect of eroding the time slack by means of VDD variation (typically, VDD decrease) or by means of clock frequency variation (fmax) in a digital module can be similar. At gate level, multi-frequency simulation can be performed at low cost. However, node electric voltages, like the power supply voltage, are absent from this level of abstraction. They implicitly influence the propagation delay of logic elements. Conversely, electric-level simulation can accurately model VDD variations. However, computer resources for electric-level simulation grow fast with circuit complexity. Hence, for test purposes, it becomes attractive to perform, in the design environment:

- Multi-frequency tests, at logic level;
- Multi-VDD tests, at circuit level.

In this dissertation, as we want to evaluate the impact of a non-ideal voltage source, VDD, on circuit performance, extensive multi-VDD simulations have been carried out. When appropriate, multi-T electric-level simulations have also been performed. Basically, the goal is to demonstrate that the proposed VT-aware methodology still holds for real-world power supply voltage sources, leading to enhanced tolerance to VT variations, while keeping performance and testability features. Multi-VDD BIST is also experimented.

### 3.3. Simulation Set-up

In a real-world on-chip environment, the power supply voltage cannot be accurately modeled by an ideal voltage source, VDD. For each power supply domain (an island in the power grid), a network of conductive layers (metal lines) is distributed on the chip. These are low resistance conductive paths, but they are not zero-resistance paths. Copper has been selected to substitute Aluminum, due to its lower sheet resistance. However, low VDD and high-performance logic circuitry leads to high current peaks, and high power density, which increases temperature and thus, metal sheet resistance. These IR voltage drops in the power grid must be taken into account when operation is performed close to its maximum frequency. Moreover, dynamic parasitic effects (capacitive and inductive) in the power grid may also have to be taken into account, depending on circuit frequency of operation. These are distributed effects. In order to constrain the simulation costs, lumped models need to be devised.

#### 3.3.1 Circuit and Power Supply Modeling

Let us consider a static CMOS digital CUT, and a local power and ground network, for which, as a first assumption, only resistive parasitics are relevant. The metal conductive layers exhibit a typical technology-dependent sheet resistance, RSH. According to the physical layout of the local power grid, resistive paths may be modeled as an equivalent resistance R in series with the ideal voltage source, VDD. Power supply current, iDD(t), feeding gate logic switching, is a pulse waveform which induces an ohmic voltage drop (IR voltage drop) [39], degrading circuit performance.

Circuit-level simulation of large digital modules can easily become prohibitive, as module complexity increases. Hence, in our modeling effort, we want to use a low-complexity CUT. If this is the case, the limited current introduces very small IR drop; hence, this effect becomes marginal. In reality, the local power network
feeds many digital modules, leading to a significant $i_{DD}$ peak current, and to a relevant IR drop. In terms of a lumped model, this can roughly lead to the circuit depicted in Figure 7. Here, we assume, for simplicity, that all digital modules, $\text{CUT}_i$, are similar, and that all resistance paths in the power grid are similar, with $R$ value. The DC ideal voltage value is $V_{\text{SET-UP}}$.

![Figure 7- Equivalent circuit for a cluster of $n$ CUT powered by a given local power network.](image)

As we move from the final $\text{CUT}_n$ to the first $\text{CUT}_1$, the voltage level increases from $V_{\text{CUT}}$ up to $V_{DD}=V_{\text{SET-UP}}$. Although $V_{\text{CUT}_i}$ are variable, let us assume that $i_{\text{CUT}_i}$ are similar. Hence, the current flowing in resistances $R$ are approximately $i_{\text{CUT}_i} = 2i_{\text{CUT}}$, $3i_{\text{CUT}}$ and so on. As a consequence, $(V_{DD}-V_{\text{CUT}})$ can be estimated as

$$V_{DD} - V_{\text{CUT}} \approx (1 + 2 + 3 + \cdots + n)RI_{\text{CUT}} \approx \left(\sum_{i=1}^{n} i\right)RI_{\text{CUT}}$$

This equation can also describe the Kirchhoff voltage law of a more lumped circuit, which we refer in this work as the set-up circuit.

### 3.3.2 Proposed Set-up Circuit

In order to assess the influence of $V_{DD}$ variations on the timing behavior of a digital $\text{CUT}$, in the context of a non-ideal voltage source, $V_{DD}$, the basic set-up circuit proposed in this work is depicted in Figure 8. In this circuit, $V_{\text{CUT}}$ represents the effective power supply voltage applied to the $\text{CUT}$, which modulates its timing response. It can assume different values and waveforms. $I_{\text{CUT}}$ is the supply current fed to a single $\text{CUT}$ and $G$ is the gain factor of $I_{\text{CUT}}$. This current source represents the loading effect of the remaining $\text{CUT}$ on $V_{\text{CUT}}$, assuming that $n$ identical (or similar) $\text{CUT}$ are powered by $V_{\text{SET-UP}}$. With the set-up circuit it is possible to study the effect of $V_{DD}$ variations on $\text{CUT}$ performance without disregarding the remnant circuit. Hence, the current-controlled current source ($G.I_{\text{CUT}}$) represents a number of $\text{CUT}$’s being approximately (and simultaneously) fed by $V_{\text{SET-UP}}$. As seen from Figure 8, $(V_{DD}-V_{\text{CUT}}) = (G + 2).R.I_{\text{CUT}}$. Comparing with the above equation, yields

$$G = \left(\sum_{i=1}^{n} i\right) - 2$$
Figure 8- Proposed lumped setup circuit

Hence, G=100 corresponds approximately to 14 identical CUT. Of course, this simplified circuit only represents the dynamic behavior of a complex digital circuit within a certain accuracy level. Each CUT exhibits its own capacitive parasitics, which modulates $i_{\text{CUT}}=i_{\text{CUT}}(t)$, the power supply current pulse. In fact, capacitive effects are implicitly considered in each CUT, through $i_{\text{CUT}}(t)$. However, the distributed effect of the RC network is modeled only in an approximate way, in the lumped model (by means of G, R parameters). Propagation delays in the power network may increase pulse widths. Moreover, when inductive effects in the power lines are considered, distributed RLC effects may be modeled with limited accuracy. Nevertheless, circuit simulations carried out with the distributed (Figure 7) and lumped (Figure 8) circuits, for a typical CUT, prove that although the exact waveform of $V_{\text{CUT}}(t)$ may slightly differ, the impact $V_{\text{DD}}$ variations on CUT signal propagation delays are modeled with good accuracy. This is due to the fact that the average values of $V_{\text{CUT}}$ in the distributed and lumped circuits are very similar. Hence, ripple in PSN (power supply noise) is modeled with low accuracy. However, the impact of PSN on delay variations is modeled accurately with the proposed set-up circuit, allowing fast circuit-level simulation, (G, R) parameters model the complexity (G) of the digital module fed by the local power grid, and its non-ideality (R). The average value of $V_{\text{CUT}}$ in a simulation performed with 14 CUT’s and the circuit depicted in Figure 7 is $V_{\text{CUT}} = 2.4$ V. Performing a simulation with the proposed test set-up circuit (Figure 8) and G=100, $R=5\,\Omega$, the corresponding average voltage value is $V_{\text{CUT}}=2.39$ V. Hence, the proposed test set-up circuit gives a correct estimation in terms of average values.

Thus, in order to study the effect of $V_{\text{DD}}$ variations on the CUT performance, extensive simulations of the set-up circuit have been carried out. This circuit has two parameters, G and R. G maps circuit complexity, while R describes the non-ideality of the local power grid.

In real-world IC, power supply voltage (connected from the outside to the chip at various supply pins) exhibits other non idealities, besides a resistive voltage drop due to a finite interconnection resistance. Typically, inductive effects cannot be neglected for high-performance IC, as high frequency power supply currents occur. These effects can be modeled by a lumped inductor, L, added in series with the ohmic resistance R in the set-up circuit, as shown in Figure 9.

Figure 9- Set-up circuit with an inductor element, L.
Moreover, inductive effects in the power network are added. All these parasitic effects are lumped and added in the positive $V_{DD}$ line. If we introduce them in the ground line, then ground bounce effects can be observed. Several combinational, pipeline and sequential circuits have been used as CUT. The case studies are described below.

### 3.3.3 Test Vectors

In order to demonstrate the effectiveness of the VT aware methodology, in the presence of non-ideal voltage sources, it is necessary to stimulate the CUT with test vector sequences that allow the activation of the critical paths, and the activation and propagation of delay faults. Test pattern generation [16] is a discipline out of the scope of the present work. For Built-In Self Test (BIST), low cost hardware TPG (like LFSR) generates pseudo-random test patterns [31]. Test pattern generation for delay faults require typically sequences of vector pairs, one initialization vector, and one activating vector, to allow the propagation of a Boolean difference (between the fault-free and the faulty circuit) through the critical path [19]. Although primitive polynomials can allow the generation of $(2^n-1)$ vectors ($n$ bit word), the unique sequence of these vectors cannot guarantee CP activation, or 100% delay fault coverage. Typically, results show that 60-70% of these faults can be covered by a LFSR-based test [4].

In this work, both pseudo-random and deterministic test patterns have been used. When pseudo-random test patterns are used, care has been taken, in order to make sure that CP are activated in the test sequence. Fault injection, to demonstrate that the VT-aware methodology does not compromise delay fault detectability, is only carried out in such a way that delay faults disturb the CP propagation delay.

In order to make result analysis easier, the output responses of the CUT have been observed either on simple memory elements, or compressed in TAE (Test Answer Evaluators) structures, like MISR, which is routinely done in BIST solutions. Output signatures (digital words) have been converted in decimal, so results could be more readable.

### 3.4. Case Studies

#### 3.4.1 Xtran

The Xtran module is a typical combinational digital circuit of a TECMIC industrial design for a fleet management system [40]. It contains several overlapping I/O combinational cones\(^5\). In this work, both the entire Xtran module and one of its dependence cones, that we refer as the Xtran block, have been used. The overall Xtran module has 8 output cones, one of which exhibits the longest propagation delay path. We refer it as the Xtran critical cone. One additional output cone was used as case study (the Xtran block), in two architectures: the original one, part of the Xtran module ($Xtran.v1$ cone), and one modified version ($Xtran.v2$ cone), for reasons that will be explained bellow.

\(^5\) A cone is a multi-input, single output combinational circuit. It can also be referred as output cone.
The overall Xtran module has 13 inputs and 8 outputs (in Annex). This digital module, tested for a relatively long set of test vectors (i.e., for many clock cycles), requires considerable computer resources for circuit-level simulation. In order to restrict simulation time, the critical path was first identified and activated, in order to highlight the $V_{DD}$ variation effect. The output cone containing the Xtran module critical path is referred as the Xtran critical cone.

3.4.1.1 Xtran Critical Cone

The Xtran’s critical path is highlighted in Figure 10 (starting at I11, PSN1N, ending FDCS0, I20). The critical cone exhibits 8 inputs. We assume that each input is driven by the output of a D-FF, and the output is captured by another D-FF. The Xtran critical path starts at the I11 line, and ends at the I20 line. I11 is the third input of a three input NAND gate. Hence, by activating this path, the switching activity imposed by I11 will take more time to propagate to the output response of the NAND gate than I10 or I12 transitions. Therefore, the maximum frequency of operation is determined by this path.

In order to activate the critical path, I1, I2, I4, I7, I9, I10, I12 and I13 input signals were hold at high state (logic ‘1’) I3, I5, I6 and I8 were hold at low state (logic ‘0’). Critical path activation is carried out by switching I11 from ‘0’ to ‘1’.

![Figure 10- Critical path of the XTRAN circuit.](image)

3.4.1.2 Xtran.v1 Cone

The Xtran block is a typical combinational cone of this industrial design, with 7 inputs and 1 output. The original Xtran block (hereafter referred as Xtran.v1) exhibits limited activity at its output. This is due to the 3-input NAND gate (see Figure 11). In fact, only one out of eight possible input vectors drive G5 to logic ‘0’. Hence, G5 shows limited switching activity, which severely limits the activation of many signal paths in the cone.
3.4.1.3 Xtran.v2 Cone

Hence, a second version of the Xtran block was implemented (hereafter referred as Xtran.v2). As shown in Figure 12, Xtran.v2 differs from Xtran.v1 only by the NOR3 gate, substituting the NAND3 gate.

After analyzing the circuits the circuit critical path was identified. For Xtran.v1 and Xtran.v2, the critical path corresponds to the $X_6-G_5-G_6-Q$ path.

3.4.1.4 Pipeline and Compacted Signature Versions

In the experiments, the Xtran block has been used driven by a pseudo-random test pattern generator (a 7 register LFSR). Initially, its output response has been compacted by a 7-register MISR. Then, a register is added at the output, between the Xtran.v1 cone and the MISR\(^6\), in order to investigate if timing failures are caused by the combinational block’s failure, or by the signature analyzer’s block, as shown on Figure 13.

---

\(^6\) The ‘MISR-like’ structure is used to compress the set of responses in the successive clock cycles. Time compression, in this case, is performed for a single input. In the Xtran module, the TAE structure is really a multi-input shift register.
3.4.2 B06 Sequential ITC’99 Benchmark with Scan

The CUT used to test the proposed dynamic scan BIST methodology is the ITC’99 B06 benchmark, which is a sequential circuit [41]. The benchmark circuit is previously synthesized with Synopsys™ (option: area optimization) and reconfigured for scan chain insertion. The structural implementation (at gate level) is shown in Figure 14.

![Figure 14- Optimized B06 CUT with scan chain.](image)

3.5. Search Space

In order to demonstrate the usefulness of the methodology, a set of design and operation variables have been used. These variables are:

- The CUT (combinational, pipeline, sequential)
- The TPG circuitry (LFSR, or other (deterministic vectors))
- The TAE circuitry (register, MISR, etc.)
- The set-up circuit (single, multiple CUT)
- The overall DUT (Device Under Test) (CUT, TPG, TAE, etc.) version: original (no DDB insertion), or modified (using the VT-aware methodology)
- DDB insertion technique: manual, or using DyDA tool
- The overall DUT state: fault-free, or defective (bridging faults)
- The power supply voltage source (ideal, R and L effects)
- The DUT temperature

The search space is illustrated in Figure 20. The key parametric variables (G, R and L) range is as follows: (G, R) with \( G \in (0, 100) \) and \( R \in (0, 5) \, \Omega \). Then, (G, R, L) with the same (G, R) range and with \( L \in (1, 100) \) nH. Physical defects tested are single resistive BRI (bridging) faults between two logic lines, disturbing the critical path.
Figure 20 – Search space to demonstrate the usefulness of the methodology.
4. Impact of the Non-Ideal Power Supply Voltage on Timing Behaviour

As IC technology scales to nanometer resolution, and functional density continues to increase, the sensitivity of the digital circuitry to power supply noise (PSN) effects continues to increase [39]. The purpose is to evaluate the impact on non-ideal power supply voltage on circuit performance, to, latter on, evaluate how the VT-aware design methodology helps to restrict this impact.

4.1. Ideal Voltage Source $V_{DD}$

The goal of this first set of experiments is to understand circuit behavior under a constant (and ideal) power supply voltage, in order to compare it with the one obtained with a non ideal voltage source, and in general with variable $V_{DD}$. As specified in section 2.2.3, $V_{DD}$ variations have an important impact on circuit performance. When an integrated circuit (IC) operates in the presence of PSN, circuit delays are disturbed. Typically, $V_{DD}$ decreases and delays increase. Hence, circuit response will be slower than under normal operating conditions. For high performance IC, operating with tight time slacks, slower circuit response may lead to a functional error, as incorrect logic values are captured by memory elements.

In order to demonstrate this effect, circuit-level simulations were performed, using the Xtran module as circuit under test (CUT) [15]. When the VT aware methodology is used, DDB insertion is implemented according to DyDA data. Xtran module, tested for a relatively long set of test vectors (i.e., for many clock cycles), requires considerable computer resources for circuit-level simulation. The CP is identified by PrimeTime™ in the Xtran critical cone (section 3.4.1.1). A limited set of test vectors was chosen to make sure that the critical path is activated, in order to highlight the effect of $V_{DD}$ variation on timing performance.

The first set of experiments was performed with an ideal DC voltage source to represent a constant power supply voltage, $V_{DD}$. The nominal $V_{DD}$, for the 350 nm AMS CMOS technology, is $V_{DD_{nom}}=3.3$ V. We assume a time slack allowing correct behavior down to 90% of $V_{DD_{nom}}$. Hence, experiments are carried out with $V_{DD}=3.0$ V.

For the Xtran module with $V_{DD}=3.0$ V and a clock frequency of 100 MHz (period of 10 ns), typical waveforms (CLK, I20, FDCS0, PCSIN and I11 lines) are shown in Figure 15 (input: I11, cone output: FDCS0, CME output: I20). At this clock frequency, the correct performance is achieved. As shown, the switching activity of I11 node produces a complementary response in I20 node in the third clock cycle rising edge. In order to identify the maximum clock frequency, $f_{max}$, for which correct operation occurs, additional circuit-level simulations were performed with variable clock frequency. For $V_{DD}=3.0$ V, circuit simulations show that $f_{max}=632.9$ MHz (clock period of $\tau_0=1.58$ ns). The corresponding waveforms are shown in Figure 16. For higher clock frequencies (e.g., for $f=636.94$ MHz, clock period of 1.57 ns), the circuit response is no longer correct, as shown in Figure 17. At this frequency, the combinational circuit still presents the correct waveform response. However, the CME that registers FDCS0 (to transfer it to the I20 node) doesn’t capture the correct logic value, leading to an output signal which is stuck-at low after the third clock.
Figure 15 - Typical waveforms for Xtran critical path with 100 MHz clock frequency.

Figure 16 - Typical waveforms for Xtran critical path with $f_{\text{max}}=632.9$ MHz clock frequency.

Figure 17 - Typical waveforms for Xtran critical path with $636.94$ MHz clock frequency ($f>f_{\text{max}}$, incorrect response).
Additional experiences were performed, to compute the propagation delay of the critical path in the combinational part of Xtran. Experiments were carried out for a constant $V_{DD}$ value of 3.0V, measuring the delay between FDCS0 and PCS1N signals (cone active output and input, respectively), for variable clock frequency. The measured Low-to-High (LH) and High-to-Low (HL) delay is shown in Figure 18.

![Figure 18- Instant of delay capture and correspondent values for a constant $V_{DD} = 3.0V$ and $f = 632 MHz$.](image)

4.2. Power Noise: Non-ideal $V_{DD}$ (IR Drop)

In order to apply a non-ideal voltage source, $V_{DD}$, the simulation set-up circuit described in section 3.3.2 was considered. Additionally, in the following experiments, a DDB cell was inserted in the clock signal path of the CME (the register at the output of the Xtran critical cone, identified by DyDA). These experiments allow us to ascertain the effects of the non-ideality of the power voltage source, and the benefits of allowing time borrowing to increase circuit tolerance to $V_{DD}$ voltage drops. In fact, without the insertion of this DDB cell, circuit behavior isn’t the correct one (for $G=100$, $R=5\Omega$). The insertion of the DDB cell, delaying the clock signal driving the flip flop providing the I20 output enhances the range of $V_{DD}$ variations for which correct behavior holds. After these modifications, the circuit was tested under the following conditions:

- $V_{DD} = 3.0V$, $G = 100$, $R = 5\Omega$, $f \in (100 MHz, f_{max})$, $T = 27^\circ C$.

First the circuit was tested at $f=100 MHz$ and performed correctly (Figure 19). In this figure, clock and clock2 signals (clock signal at the output of the DDB cell) are overlapped. Now, the presence of power noise is visible, as $V_{CUT} < V_{DD}$. The $V_{CUT}$ waveform is shown in Figure 20, where it is possible to observe voltage ripple due to clock switching and the correspondent transitions in the circuit flip-flops. The average $V_{CUT}$ value is lower than the ideal power supply voltage ($V_{DD}=3.0 V$), as expected ($V_{CUTave}=2.90 V$).
Then, simulations up to $f = f_{\text{max}}$ were carried out. Now, with a non-ideal power supply voltage source, $f_{\text{max}} = 689$ MHz (period of 1.45ns) which is higher than the value obtained for the circuit without PSN. Why? DDB insertion increases circuit tolerance. The waveforms obtained with $f_{\text{max}} = 689$ MHz are shown in Figure 21. At this frequency and in the presence of power noise, $V_{\text{CUT}}$ waveform is as shown in Figure 22.
Figure 21- Typical waveforms for Xtran critical path with $f_{\text{max}} = 689$ MHz in the presence of PSN, $(G, R) = (100, 5 \ \Omega)$.

Figure 22- Typical $V_{\text{CUT}}$ waveform in the presence of PSN obtained with $f_{\text{max}} = 689$ MHz $(G, R) = (100, 5 \ \Omega)$.

Figure 23 shows the waveforms for $f=714$ MHz (period of 1.4ns). As $f>f_{\text{max}}$, an error due to excessive delay in the combinational circuit occurs. The clock period, $V_{\text{CUT}}$ voltage variation, $\Delta V_{\text{CUT}}$, average $V_{\text{CUT}}$ values are shown in Table 1.

<table>
<thead>
<tr>
<th>Period (ns)</th>
<th>$\Delta V_{\text{CUT}}$ (V)</th>
<th>Average $V_{\text{CUT}}$ (V)</th>
<th>LH Delay (ns)</th>
<th>HL Delay (ns)</th>
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</thead>
<tbody>
<tr>
<td>10.0</td>
<td>0.523</td>
<td>2.90</td>
<td>0.66</td>
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<td>1.4</td>
<td>0.33</td>
<td>2.45</td>
<td>0.73</td>
<td>1.24</td>
</tr>
</tbody>
</table>

Table 1- Set of values achieved for Xtran in the presence of power noise.
4.3. Power Noise: Non-ideal $V_{DD}$ (with $R$, $L$ Effects)

Non-ideality due to inductive effects has also been evaluated, using the Xtran module as CUT, and the modified set-up circuit previously depicted in Figure 9.

Simulation conditions are as follows.

- $V_{SET-UP} = 3.0$ V, $G = 100$, $R = 5\ \Omega$.
- $L = 1$, 10 and 100 nH, $f \in (100$ MHz, $f_{max})$, $T = 27^\circ$ C.

4.3.1 $L = 1$ nH

At $f=100$ MHz and $L=1$ nH, the circuit behavior is very similar to the obtained without inductive effects. The main difference is in the $V_{CUT}$ waveform that exhibits stronger ripple, as shown in Figure 24. This is to be expected, as an additional voltage component, $(L\ di/dt)$, is present.

Under the assumptions, $f_{max}$ is again 689 MHz (period of 1.45ns), like in the case without the inductor ($L=0$). The correspondent waveforms are presented in Figure 25. The $V_{CUT}$ waveform is presented in Figure 26.
The V\textsubscript{CUT} values and the delays are presented in Table 2. The time frame is higher in Figure 25, in order to better compare the differences between different values of L. For \(f > f_{\text{max}}\), namely for \(f = 714\) MHz (period of 1.4 ns) the waveforms are shown in Figure 27. Again, the combinational circuit is the first to fail, being this error passed through the flip flop and imposed at I20.

<table>
<thead>
<tr>
<th>Period (ns)</th>
<th>(\Delta V_{\text{CUT}}) (V)</th>
<th>Average (V_{\text{CUT}}) (V)</th>
<th>Delay LH (ns)</th>
<th>Delay HL (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.0</td>
<td>0.61</td>
<td>2.90</td>
<td>0.67</td>
<td>1.01</td>
</tr>
<tr>
<td>1.45</td>
<td>0.33</td>
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<td>0.4</td>
<td>2.46</td>
<td>0.74</td>
<td>1.23</td>
</tr>
</tbody>
</table>

Table 2- Set of values obtained for Xtran in the presence of power noise and \(L=1\) nH.

Figure 25- Typical Xtran waveforms in the presence of power noise for \(f=689\) MHz and \(L=1\) nH.

Figure 26- \(V_{\text{CUT}}\) waveform of in the presence of power noise for \(f=689\) MHz and \(L=1\) nH.
4.3.2 \( L = 10 \text{ nH} \)

For \( L = 10 \text{ nH} \), circuit behavior is very similar to the one for \( L = 1 \text{ nH} \). For \( f = 100 \text{ MHz} \), \( V_{\text{CUT}} \) waveforms are shown in Figure 28. Now, clock2 waveform presents overshoot. The maximum frequency for \( L = 10 \text{ nH} \) is equal to the one obtained for \( L = 1 \text{ nH} \). The effect of enhanced \( V_{\text{DD}} \) tolerance due to DDB insertion still holds, in the presence of inductive PSN. For \( f_{\text{max}} = 689 \text{ MHz} \) circuit waveforms are presented in Figure 29. Faulty behavior is visible for \( f = 714 \text{ MHz} \), as depicted in Figure 30. Relevant \( V_{\text{CUT}} \) data for this case is presented in Table 3.

<table>
<thead>
<tr>
<th>Period (ns)</th>
<th>( \Delta V_{\text{CUT}} ) (V)</th>
<th>Average ( V_{\text{CUT}} ) (V)</th>
<th>Delay LH (ns)</th>
<th>Delay HL (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.0</td>
<td>0.837</td>
<td>2.90</td>
<td>0.72</td>
<td>1.13</td>
</tr>
<tr>
<td>1.45</td>
<td>0.44</td>
<td>2.44</td>
<td>0.73</td>
<td>1.25</td>
</tr>
<tr>
<td>1.4</td>
<td>0.48</td>
<td>2.45</td>
<td>0.73</td>
<td>1.22</td>
</tr>
</tbody>
</table>

Table 3- Set of values obtained for Xtran in the presence of power noise and \( L = 10 \text{ nH} \)

![Figure 27- Typical Xtran waveforms in the presence of power noise for \( f = 714 \text{ MHz} \) and \( L = 1 \text{ nH} \).](image)

![Figure 28- Waveform of \( V_{\text{CUT}} \) in the presence of power noise and \( L = 10 \text{ nH} \) for a frequency of 100 MHz.](image)
4.3.3 $L = 100 \text{ nH}$

Similar behavior under extreme conditions ($L=100 \text{ nH}$) were observed by circuit simulation. Results for $f=100\text{MHz}$ (period of 10ns) are shown in Figure 31 (correct behavior). The corresponding $V_{\text{CUT}}$ waveform is shown in Figure 32.

The maximum frequency is $f_{\text{max}}=666 \text{ MHz}$ (period of 1.5ns) and the circuit response at this frequency is shown in Figure 33. The correspondent $V_{\text{CUT}}$ response is illustrated in Figure 34.

For $f>f_{\text{max}}$, namely for $f=689 \text{ MHz}$ (period of 1.45ns), the circuit response is incorrect as shown in Figure 33 as well as the $V_{\text{CUT}}$ response is presented in Figure 34. Relevant $V_{\text{CUT}}$ values and delay are presented in Table 4.
<table>
<thead>
<tr>
<th>Period (ns)</th>
<th>$\Delta V_{\text{CUT}}$ (V)</th>
<th>Average $V_{\text{CUT}}$ (V)</th>
<th>Delay LH (ns)</th>
<th>Delay HL (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.905</td>
<td>2.91</td>
<td>0.69</td>
<td>1.04</td>
</tr>
<tr>
<td>1.5</td>
<td>0.34</td>
<td>2.46</td>
<td>0.73</td>
<td>1.23</td>
</tr>
<tr>
<td>1.45</td>
<td>0.376</td>
<td>2.43</td>
<td>0.74</td>
<td>1.28</td>
</tr>
</tbody>
</table>

Table 4- Set of values obtained for $X_{\text{tran}}$ in the presence of power noise and $L=100$ nH

- Figure 31- Typical waveforms in the presence of power noise for $f=100$ MHz and $L=100$ nH.

- Figure 32- Waveform of $V_{\text{CUT}}$ in the presence of power noise for $f=100$ MHz and $L=100$ nH.
Figure 33- Typical waveforms in the presence of power noise for a $f=666$ MHz and $L=100$ nH.

Figure 34- Waveform of $V_{\text{CUT}}$ in the presence of power noise for a $f=666$ MHz and $L=100$ nH.

Figure 35- Typical waveforms achieved in the presence of power noise for a $f=689$ MHz and $L=100$ nH.
4.4. Conclusions

In this chapter, the analysis of non-ideal power supply voltage on digital circuit performance was performed, using a set-up circuit emulating multiple Xtran modules with single DDB insertion in the clock signal driving the D-FF capturing the output signal of the critical cone. Non-ideality of the voltage source considered IR drop, and inductive effects. Clearly, PSN induces voltage ripple and lower average $V_{\text{CUT}}$ values. Voltage ripple does not induce a significant effect, either on Boolean response, or on timing response. The main effect is due to the drop of the average value of $V_{\text{CUT}}$, which, in the simulated example, was in the order of 17% (0.5 V on 3.0 V). Results demonstrated that the VT-aware methodology holds in the presence of non-ideal voltage source, at least for this case study, which is encouraging. DDB insertion still enhances circuit tolerance to $V_{\text{DD}}$ variations. The following Figures summarize the results.

Average $V_{\text{CUT}}$ voltage variation with $(f, L)$ is presented in Figure 36. Both power noise and frequency degrade $V_{\text{CUT}}$. In Figure 36, “Initial” stands for ideal $V_{\text{DD}}$ voltage source. For higher frequencies, the average value of the $V_{\text{CUT}}$ voltage decreases around 20%.

PSN induces average power supply voltage drop. The $\Delta V_{\text{CUT}}$ is shown in Figure 37.

![Figure 36- Average $V_{\text{CUT}}$ values ($V_{\text{CUTave}}$) for circuits with and without power noise.](image)

![Figure 37- $V_{\text{CUT}}$ voltage variations ($V_{\text{CUT}}$ ripple).](image)
The LH and HL delay variations, due to the non-ideality of $V_{DD}$, are depicted in Figure 38 and Figure 39, respectively. Similar conclusions can be drawn, due to a significant drop on the average value of $V_{CUT}$.

Figure 38-Delay achieved for the low/high transitions.

Figure 39- Delay achieved for the high/low transitions
5. VT-aware Methodology with Scan Design

The purpose of this chapter is to assess (although, in a limited way) how the use of the VT-aware design methodology in sequential circuits, designed with scan, is viable or not. The Torino ITC’99 benchmark circuit, B06, designed with scan, is used as CUT in two architectures: original scan B06 [41] (without DDB insertion) and modified (with DDB insertion, proposed by the DyDA tool). In this case the longest paths are in the circuit registers, not only in the clock but also in data path. Simulations were performed in two abstraction levels, logic and electric. Logical simulations were carried out with \textit{Verilog XL}. Circuit-level simulations were performed with \textit{Virtuoso Spectre}. The original scan B06 circuit is shown in Figure 14, at gate level. In all circuit-level simulation results presented in this chapter, $V_{\text{SET-UP}}$ (Figure 9) was defined as 90% of $V_{\text{DDnom}}=3.3$ V (for this IC technology), guaranteeing a reasonable time slack at $V_{\text{DDnom}}$.

5.1. Logic-level Simulation

First, logic level circuit description (in Verilog) is used by DyDA and \textit{PrimeTime}$^{\text{TM}}$ to identify the critical paths, and propose DDB insertion. Two short delay data paths are identified (primary inputs), requiring DDB insertion. In order to introduce time borrowing, and thus enhance tolerance to VT variations, one additional DDB is inserted to delay the clock signal of three (out of nine) registers. Logic-level simulations were also performed with Verilog X$^{\text{TM}}$.

Results for the B06 scan benchmark are summarized in Table 5. As expected, the use of the VT-aware design methodology leads to a performance improvement, estimated as 2.98%. Note that this estimate is made for nominal $V_{\text{DD}}$ (as the delay parameters in the AMS 350 nm CMOS cell library are computed for nominal conditions) and use no layout information. The estimate also computes the overhead (in silicon area and power consumption). As this is a simple benchmark circuit, the overhead is significant. For complex digital modules, the overhead tends to decrease (as it happens in BIST solutions). The modified circuit presents a 6.62% area overhead, 18% dynamic power overhead and 7% leakage power overhead. As it is based on static timing analysis, these results are independent on the applied test vectors.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Original Circuit</th>
<th>Modified Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>B06 with scan</td>
<td>43</td>
<td>6857.2</td>
</tr>
</tbody>
</table>

Table 5- Logical results obtained (Synopsys, DyDA) for B06 with scan.
5.2. Circuit-level Simulation

The scan B06 circuit can work in two operating modes, the normal and the scan mode. The circuit block diagram is depicted in Figure 40. The circuit has 9 flip-flops (thus, introducing 9 SI and 9 SO), 34 logic gates, 2 PI and 2 PO. DyDA did not identify any critical path between the I/O of the feedback registers, which allow us to apply the VT-aware methodology.

In the normal operating mode (test select, or \( \text{test} \_\text{se} = '0' \)), some stimuli are imposed to \( \text{eql} \) and \( \text{cont} \_\text{eql} \) primary inputs. When the circuit operates in scan mode (\( \text{test} \_\text{se} = '1' \)), some stimulus are applied to \( \text{test} \_\text{si} \) (scan input).

The observable outputs in normal mode are the \( \text{cc} \_\text{mux} <2:1> \) and in the scan mode are the \( \text{uscite} <2> \) (scan out).

In order to perform a complete evaluation of the effectiveness of the modified circuit, it is necessary to identify all critical paths (within a user’s specified range), usually with delays \( \tau \in (0.9; 1.0) \) \( \tau_0 \) (the longest signal propagation delay). Then, test pattern generation should be carried out, generating the test vector pairs which are able to activate and propagate these critical paths. For a sequential circuit (the scan B06 in normal mode of operation), this is a cumbersome process. For the scan B06 in test mode, the test patterns need to be expanded to perform the shift-in (9 clock cycles, associated to the 9 registers in the scan chain), test application, test response capture and shift-out (again, 9 clock cycles). This implies a long test length (many test vectors), and thus a huge computational cost in circuit-level simulation. As test pattern generation is out of the scope of this work, a decision was made to apply a limited set of test vectors to perform (1) \( f_{\text{max}} \) computation and (2) the comparison of the multi-\( V_{\text{DD}} \) time response of the original and modified B06 circuits.

5.2.1 Normal Mode

5.2.1.1 Ideal Voltage Source \( V_{\text{DD}} \)

In the first experiment, the circuit was simulated under the following conditions.

- \( V_{\text{DD}} = 3.0V \), \( f = 100 \text{ MHz} \), \( T = 27^\circ C \).

Results for the normal operating mode are illustrated in Figure 41. These results are the ideal ones, obtained at low frequency (\( f=100 \text{ MHz} \)), in order to guarantee the correct result. These waveforms are used as
reference to compare with the waveforms obtained in the presence of power supply noise. These results were achieved for a single clock circuit.

5.2.1.2 Power Noise: Non-ideal \( V_{DD} \) (IR Drop)

PSN is simulated using a non-ideal \( V_{DD} \) source and the set-up circuit described in 3.3.2. When the power noise is thus introduced, the original B06 scan circuit provides erroneous responses. Hence, the circuit was analyzed with DyDA, in order to improve circuit’s tolerance to \( V_{DD} \) variations. DyDA performs a blind analysis of the circuit, in the sense that DyDA does not consider the operation mode. Critical paths are identified and DDB cells are introduced. Following every DDB insertion, a new static timing analysis is performed and short paths are identified and fixed. In the modified B06 scan circuit, three DDB cells are inserted, one in the clock line, and two in signal lines: one for the test_se and other for eql.

With the modified B06 scan as CUT and the test set-up circuit, simulations were performed, under:

- \( V_{DD} = 3.0V \), \( f = 100 \text{ MHz} \), \( T = 27^\circ \text{ C} \).
- \( G=100 \), \( R=5\Omega \).

The resulting waveforms are similar to the ones presented in Figure 41, with some noise. The \( V_{CUT} \) waveform is presented on Figure 42. The average \( V_{CUT} \) value is 2.90 V.

In order to test circuit tolerance to power noise, the clock frequency was increased, leading to a \( V_{CUT} \) average value decrease. The lowest \( V_{CUT} \) average value that guarantees correct circuit behavior is 2.63 V, with a ripple voltage of 0.72 V. The correspondent waveform is presented in Figure 43.
5.2.1.3 Power Noise: Non-ideal $V_{DD}$ (with R and L Effects)

Using the test set-up circuit shown in Figure 9, with an additional parasitic inductor, L, additional simulations were performed. Results are similar to the ones without the L effect.

Simulations were performed under the following conditions:

- $V_{DD} = 3.0\, \text{V}$, $f = 100\, \text{MHz}$, $T = 27^\circ \text{C}$.
- $G = 100$, $R = 5\, \Omega$, $L = 10\, \text{nH}$.

Again, the clock frequency was increased. The minimum average $V_{CUT}$ value leading to correct circuit behavior is identical to the one without L. The difference is in the voltage ripple, now yielding a value of 1.18 V. The waveforms are presented on Figure 44.
5.2.2 Scan Mode

5.2.2.1 Ideal Voltage Source $V_{DD}$

In the first experiment, the circuit was simulated under the following conditions.

- $V_{DD} = 3.0V$, $f = 100$ MHz, $T = 27^\circ$ C.

The analyzed input is $test\_si$ and the output is $uscite<2>$. The resultant waveforms that are used as a reference are presented on Figure 45.

5.2.2.2 Power Noise: Non-ideal $V_{DD}$ (IR Drop)

Power noise is introduced in the modified B06 scan circuit specified in 5.2.1.2. Simulations were performed under the following conditions:

- $V_{DD} = 3.0V$, $f = 100$ MHz, $T = 27^\circ$ C.
- $G=100$, $R=5\Omega$. 

Figure 44- $V_{CUT}$ waveform obtained with power noise ($L = 10$ nH).

Figure 45-Typical waveforms for B06 scan circuit, operating in scan mode ($f=100$ MHz).
The resulting waveforms are similar to the ones presented in Figure 45, only with some noise. The \( V_{\text{CUT}} \) waveform is presented on Figure 46. The average \( V_{\text{CUT}} \) value is now 2.89 V. The clock frequency is increased. The highest \( V_{\text{CUT}} \) average value circuit can handle without failing is 2.43V, with a ripple of 0.34V as shown on Figure 47.

![Figure 46- \( V_{\text{CUT}} \) waveform for the modified B06 it operating in scan mode](image)

![Figure 47- Maximum fault-free \( V_{\text{CUT}} \) waveform of the modified B06 scan circuit in scan mode](image)

### 5.2.2.3 Power Noise: Non-ideal \( V_{\text{DD}} \) (with R and L Effects)

Recurring to the test set-up circuit (Figure 9), with an additional inductance, \( L \), new simulations were performed. Results were very similar to the ones obtained without \( L \).

Simulations were performed under the following conditions.

- \( V_{\text{DD}} = 3.0 \text{V}, f=100\text{MHz}, T = 27^\circ \text{C}. \)
- \( G=100, R=5 \Omega, L=10 \text{nH}. \)

The circuit’s minimum \( V_{\text{CUT}} \) average value is identical to the one without \( L \). The difference is in the waveform ripple, now yielding a value of 0.37V. The corresponding waveforms are presented in Figure 48.
5.3. Conclusions

Simulation results clearly indicate that enhanced tolerance to \( V_{DD} \) variations is obtained with the VT-aware design methodology, both in normal and scan modes of operation, using DyDA and the insertion of 3 DDB cells. At logic level, the overall performance improvement achieved was estimated (using STA) as 3%.

At circuit level, it was demonstrated that, for both operating modes, DDB insertion makes the B06 scan circuit more tolerant to power noise. The maximum \( V_{\text{CUT}} \) average value the circuit can accommodate, without functional error, has decreased from 3.0 V to 2.63V, which is a 12% improvement. The maximum ripple for the normal mode was 1.18 V which means that the \( V_{\text{CUT}} \) voltage have a variations from 2.05 V to 3.23V. When operating in scan mode these values decrease, presenting a maximum ripple of 0.37 V, which leads to a \( V_{\text{CUT}} \) average value from 2.26V to 2.63V.
6. Additional Results (VT Tolerance and Delay Fault Detection)

The purpose of this chapter is threefold. First, we want to consolidate previous results on the effectiveness of the VT-aware methodology in the presence of non-ideal $V_{DD}$ voltage source. This is performed by exploiting more thoroughly the search space, described in 3.5. Second, two additional issues are addressed: (1) discussion of limitations of tolerance gains, coming from the CUT itself, or from the on-chip test circuitry, and (2) demonstration that delay fault coverage, using multi-$V_{DD}$ test, can still be achieved under non-ideal $V_{DD}$ source, when the VT-aware methodology is used (although using a wider range of $V_{DD}$ values. Finally, temperature variations are simulated, in order to extend the conclusions (regarding non-ideal $V_{DD}$) to this parametric variation. Results are shown for the two Xtran blocks described in 3.4.1, namely Xtran.v1 and Xtran.v2, using manual and DyDA-driven DDB insertion.

6.1. Xtran.v1 (BIST Environment)

As referred in section 3.4.1.2, this Xtran block (one Xtran output cone) has 7 inputs and 1 output. The first experiments are performed using the DUT depicted in Figure 49. Pseudo-random test stimuli are generated by a primitive polynomial 7-bit LFSR. The Q output response is captured by the ‘MISR-like’ structure (7-bit LFSR, performing time compression of the Q output values). Note that, in this unusual configuration, the TAE (Test Answer Evaluator) structure introduces an additional delay in signal path\(^7\). In fact, the CP associated with the combinational CUT is the X6-G5-G6-Q path. However, the DUT CP is the CUT CP, augmented with the delay of the EXOR gate connected to the first FF of the TAE. CP computation is carried out by PrimeTime\(^\text{TM}\). The longest propagation delay time of the DUT is 1.93 $ns$.

6.1.1 Original Circuit

As mentioned, experiments with the original Xtran.v1 circuit have been carried out in order to assess the impact of $V_{DD}$ variations on the CUT. The DUT described above was used in a multi-DUT environment, using the set-up circuit proposed in 3.3.2.

\(^7\) In normal operation mode, the CP delay is only the one due to the combinational block. In this case, test results compression is made, at the single output CUT, in consecutive clock cycles, in a 7-bit signature.
First, the circuit clock maximum frequency was computed, using the Cadence script described in 2.4.1. Again, \( V_{\text{SET-UP}} \) was defined as 90% of \( V_{\text{DDnom}}=3.3 \text{ V} \) (for this IC technology), guaranteeing a reasonable time slack at \( V_{\text{DDnom}} \). The correct circuit signature, in decimal, is “93”. The computed value of \( f_{\text{max}} \) is 735.29 MHz \( (\tau_0=1.36 \text{ ns}) \). Simulation conditions are as follows.

- \( V_{\text{DD}} = 3.0\text{V} \), \( G = 0 \), \( R = 1 \Omega \), \( f = 735.29 \text{ MHz} \), \( T = 27^\circ \text{C} \).

The DUT has two blocks with 7 registers. Without DDB insertion, all switching activity occurs simultaneously in these registers. Delaying the clock trigger in some CME with DDB insertion, the \( i_{\text{DD}} \) peak may be lower, as not all registers switch at the same time. Typical waveforms are shown in Figure 50. These waveforms show the PSN. The major differences identified in simulation are in the order of 0.3\( V \) (\( V_{\text{CUT}} \)) and 3\( mA \) (\( i_{\text{CUT}} \)).

![Figure 50- Typical waveforms obtained with Xtran.v1 and a clock period of 1.36 ns.](image)

6.1.2 Modified Circuit (with Manual DDB Insertion)

The application of the VT-aware methodology to the Xtran.v1 DUT leads to DDB insertion. For the Dynamic Delay Buffer cell, architecture \( a_2 \) is used, as shown in Figure 51. Typical waveforms of clock and clock2 signals are shown on Figure 52.

![Figure 51-DDB cell (architecture \( a_2 \)).](image)
DDB insertion can be carried out manually by the designer, or automatically using the DyDA tool. The first set of experiments was performed with manual DDB insertion. The rationale is to assume that time borrowing for signature capture needs to be implemented. Hence, one DDB cell is inserted in the clock signal path driving all MISR flip-flops, thus providing additional time for the CUT to respond. This single DDB cell output (clock2 line) has a large fan-out, as it drives 7 D-FF cells. This increases \( \tau(V_{DD}, T) \) delay introduced by this DDB cell. Therefore, additional tolerance to VT variations is to be expected.

Under these circumstances, \( f_{max} \) is computed as \( f_{max} = 874.81 \text{ MHz} \ (\tau_0=1.14 \text{ ns}) \) for \( V_{DD}=3.0 \text{ V} \), a 16\% time improvement, as compared to the original DUT (without DDB). Typical waveforms are presented in Figure 53, for a clock period of 1.36 ns.

As expected, DDB insertion modifies I1 and VSET-UP waveforms. The main difference between Figure 50 and Figure 53 waveforms is associated to the delayed switching behavior of the MISR. However, this difference does not significantly changes timing response.

6.1.3 Parametric Variations (G, R, L)

In order to better exploit the search space, new simulations were carried out in two scenarios: (1) variable (G, R), i.e., variable complexity and IR drop, and (2) idem, plus L variation.

6.1.3.1 Original Circuit

Simulation conditions are now as follows.
- $V_{DD} = 3.0\text{V, } f = 735.29\text{ MHz, } T = 27^\circ\text{ C.}$
- G changes from 1 to 300 using a logarithmic scale, that is, steps of 10 between 0 and 100 and steps of 100, between 100 and 300.
- For each value of G, R changes between 1 and 5 $\Omega$ using steps of 1 $\Omega$.

The first result is that, for $f = 735.29\text{ MHz}$, no correct signature is obtained. This means that, in a multi-CUT circuit ($G \geq 1$), the $V_{\text{CUT}}$ degradation only allows correct operation for lower frequency. In fact for $G=100$ and $R=5\ \Omega$, $f_{\text{max}} = 333.33\text{ MHz}$ (clock period of 3.0 ns). Results are shown in Figure 54, where a $G=0.1$ value is used to simulate a single CUT environment (correct decimal signature: ‘93’).

![Figure 54- Set of signatures of the Xtran.v1 DUT for different combinations of G and R.](image1)

For the (G, R) range, $V_{\text{CUT}}$ average are depicted in Figure 55. As shown, the larger area corresponds to $V_{\text{CUTave}}$ values between 2.5 V and 3.0 V. The correspondent average currents are presented on Figure 56, and range from 0.4 to 1.5 mA. These values reflect the influence of the set-up circuit on CUT’s behavior.

![Figure 55- Average $V_{\text{CUT}}$ values of voltage achieved for the original Xtran.v1 DUT.](image2)
6.1.3.2 Modified Circuit (with Manual DDB Insertion)

With DDB manual insertion, circuit performance significantly improves (see Figure 57). In fact, for \( G \in (1, 40) \) a correct signature is now obtained for the complete \( R \) range; for \( G = 50 \), only for \( R = 5 \Omega \) an erroneous behavior is detected. For \( G \in (50, 100) \), the circuit behavior is correct only for \( R = 1 \Omega \). For \( G = 300 \), all \( R \) values lead to a circuit error, as the MISR flip-flops stuck-at logic “1111111” = decimal ‘127’.

6.1.3.3 Inductive Parametric Variations

In order to analyze Xtran.v1 DUT response to variable \( V_{DD} \), under parasitic inductance effects, the set-up circuit presented in Figure 9 was used. Original Xtran.v1 DUT circuit always leads to erroneous behavior for \( f = 735.29 \) MHz. The modified circuit, with manual DDB insertion was simulated, under the following conditions:
- V_{DD} = 3.0V, f = 735.29 MHz, T = 27º C.
- G fixed at 40, 50, 100, 200, and 300 as a frame of the previous results.
- For each value of G, R changes between 1 and 5 Ω using steps of 1 Ω.
- L = 10nH.

Results were as expected. Correct signatures are obtained for the same (G, R) range that was identified in section 6.1.3.2. No relevant difference in average voltage and current values is observed. This results from the fact that V_{CUT} waveforms with or without L are similar (although with a different ripple). In this case, correct signatures are obtained with V_{CUT} > 2.7 V and I_{CUT} < 1.406 mA.

6.1.4 – Modified Circuit (with DyDA DDB Insertion)

The original Xtran.v1 CUT was modified according to what the designer thought it would be a good solution. Is it so? A new modified version, using DyDA driven DDB insertion, was created and tested. DyDA recommends introducing a DDB cell only in the clock that feeds MISR F7, as shown on Figure 58.

With this new DDB insertion, additional simulations were performed under the same conditions described in 6.1.3.1. Now, results show an increase in circuit tolerance of 40%, far better than the manual DDB insertion version. This result highlights the fact that the DyDA is a useful tool, in the perspective of providing an excellent solution for DDB insertion.

![Figure 58-DyDA architecture for the Xtran.v1 two-phase clock](image)

6.2. Xtran.v2 (BIST Environment)

The difference between Xtran.v1 and Xtran.v2 is the 3-input (NAND or NOR) gate with X4, X5 and X6 inputs and G5 outputs, as it can be seen in Figure 49 and Figure 59. With this modification, the switching activity at the circuit output significantly increases, as illustrated on Figure 60. For the Xtran.v2 DUT, CP delay computation with PrimeTime™ yields 1.90 ns. The circuit CP also corresponds to the X6-G5-G6-Q plus the EXOR gate path, as in the Xtran.v1 circuit.
Circuit-level computation of $f_{\text{max}}$ (for $V_{DD} = 3.0V$) now leads to $= 666.66$ MHz (clock period of 1.5 ns).

6.2.1 Original Circuit

As the process is repetitive, only a subset of conditions is used in simulation. Simulation conditions are as follows:

- $V_{DD} = 3.0V$, $f = 666$ MHz, $T = 27^\circ$ C.
- $G = 40, 50, 100$ and $200$.
- For every $G$ value, $R$ changes between 1 and 5 $\Omega$ using steps of 1 $\Omega$.

As for Xtran.v1, for $f=f_{\text{max}}$ (now, 666 MHz, instead of 735.29 MHz), timing violations always occur. Hence, in a multi-CUT circuit ($G \geq 1$), the $V_{\text{CUT}}$ degradation only allows correct operation for a lower frequency. Single CUT is simulated with $G=0.1$, as shown in Figure 61, leading to correct signatures.

The $I_{\text{CUT}}$ and $V_{\text{CUT}}$ average values were computed, leading to almost equal values as the Xtran.v1 counterparts.
6.2.1 Modified Circuit (with Manual DDB Insertion)

The same manual DDB insertion was tried: one DDB cell inserted in the clock signal path driving all MISR flip-flops. The results obtained for this modified circuit were very similar to the results achieved with the manually modified Xtran.v1 circuit. The improvement in clock frequency obtained with manual DDB insertion is 15%, as now \( f_{\text{max}} = 781.25 \text{ MHz} \), for a power supply voltage of 3.0 V.

Additional simulations were carried out for the modified circuit, using the same conditions applied for the original circuit. For these conditions and, as expected, the circuit performance is very satisfactory. In fact, for all applied (G, R) combinations, the DUT exhibits a considerable increase in performance. For all the combinations achieved with a gain value of 40 and 50, the correct signature was obtained. For \( G=100 \), only the lower values of \( R \) have produce a correct signature. For a gain factor of 200 and 300, only a correct signature was obtained, for \( R=1 \Omega \). Results are shown in Figure 62. As for the original circuit, it is possible to observe a linear platform in the graph that represents the circuit correct behavior. The main difference between the modified and the original circuit is the fact that a correct signature have been obtained with \( G=50 \) and \( R=5 \Omega \) as well as for \( G=300 \) and \( R=1 \Omega \).
The I_{\text{cut}} and V_{\text{cut}} average values were computed. Correct behavior requires V_{\text{dd}} > 2.56 V and I_{\text{cut}} < 1.34 mA. Again, DDB insertion almost does not impact circuit power consumption.

### 6.2.2 – Inductive Parametric Variations

We analyzed the Xtran.v2 response to variable V_{\text{dd}}, using the set-up circuit (Figure 9). The tested version of Xtran.v2 was the modified one (with DDB), as for the original circuit response was incorrect for the (G, R) domain as reported in 6.1.3.1.

In order to observe the CUT behavior with inductive parametric variations, simulation conditions are as follows.

- \( V_{\text{dd}} = 3.0V, f = 666 \text{ MHz}, T = 27^\circ \text{C}. \)
- G fixed at 40, 50, 100 and 200 as a frame of the previous results.
- For each value of G, R changes between 1 and 5 \( \Omega \) using steps of 1 \( \Omega \).
- L fixed at 10nH.

Results were as expected. Correct signatures are obtained for the same (G, R) combinations as identified in 6.2.1. There is not a significant difference in the average voltage and current values. These results are easily understandable, if we compare the waveforms for the set-up circuit with and without an inductor inserted in the set-up circuit. Hence, correct functionality requires V_{\text{cut}} > 2.70 V and I_{\text{cut}} < 1.39 mA.

### 6.3. Xtran.v1 and Xtran.v2 (Pipeline Environment)

Typical combinational data paths for fast data processing partition the long data paths in short ones, in a pipeline configuration. Hence, circuit functionality can be performed at higher speed, although introducing latency (i.e., taking additional clock cycles to do it). Therefore, a modification in the Xtran cones has been introduced, in order to represent them as pipeline stages.
6.3.1 Xtran.v1 as Pipeline Stage

Hence, the same pseudo-random TPG is used (7-bit LFSR), and now the typical DfT architecture (Figure 13) is used, by introducing a data capture register at the output of the Xtran.v1 bloc, as shown in Figure 63. Now, the combinational block is isolated from the TAE structure, allowing the CP to be associated only with the functional data path.

![Figure 63: Xtran.v1 with a blocking flip-flop and a MISR-like TAE.](image)

6.3.1.1 Original Circuit

First, the maximum frequency of the circuit for correct operation was identified for a power supply voltage of 3.0 V. The new computed value was $f_{\text{max}}=813 \text{ MHz}$. The decimal signature value is “30”. The computed value for the combinational block, 735.29 MHz, represents 90.44% of this new value.

For this new Xtran.v1 DUT and the set-up circuit, new simulations were performed, with

- $V_{DD} = 3.0 \text{ V}, f = 735.29 \text{ MHz}, T = 27^\circ \text{ C}$.
- G changes from 1 to 300 using a logarithmic scale, that is, steps of 10 between 0 and 100 and steps of 100, between 100 and 300.
- For each value of G, R changes between 1 and 5 Ω using steps of 1 Ω.

For these conditions, no correct signatures were obtained. A reference simulation was performed for G=0.1 (single CUT). For the whole range of (G, R) values, decimal responses are depicted in Figure 64.
6.3.1.1 Modified Circuit (with DDB insertion)

First, a DDB cell was added to the circuit in order to control the clock signal driving the MISR registers (manual DDB insertion). This situation didn’t produce any correct response. In fact, with the introduction of the additional FF, a new critical path was detected in the MISR sequence. This situation was identified using Primetime™, and highlights a significant design issue, that must be taken into account when designing DfT circuits with the VT-aware design methodology. In fact, critical paths may, in principle, belong to the functional CUT, or to the test circuitry, or to both. The path that presents the highest delay time, 1.56 ns, is shown in Figure 65 and is in the MISR structure, incorporating two XOR gates. The longest path delay produced in the combinational circuit is 1.54 ns and is illustrated in Figure 65. With this situation, many possible combinations have to be tested, in order to define where DDB insertion should take place, not only in the clock signal driving the new FF, but also in the clock paths driving the MISR FF. The selected solution was identified recurring to DyDA. The two FF, identified by DyDA, which should be driven by delayed clock signal, are the new FF and the first FF of the MISR, as shown in Figure 66.

![Figure 64-Set of signatures for the original Xtran.v1 circuit, and variable (G, R) in the pipeline environment.](image)

![Figure 65- a) Circuit path that exhibits a maximum propagation delay; b) Circuit path that exhibits a maximum propagation delay in the combinational block.](image)
With this modified circuit, a new value for $f_{\text{max}}$ was identified for $V_{\text{DD}}=3.0$ V. The correct signature, “30”, holds until $f_{\text{max}}=1052.6$ MHz (clock period of 0.95 ns). This is a 22.7% improvement, as compared to the original circuit. Simulation results are shown in Figure 67. The correct signature was obtained for all resistance values combined and for $G \in (10, 30)$. For $G \in (40, 90)$, only some of the resistance values lead to the correct signature. For $G=100$, only the $R=1 \Omega$ presents the correct signature. For correct functionality, it is necessary that $V_{\text{CUT}} > 2.78$ V and $I_{\text{CUT}} < 1.77$ mA.

6.3.1.2 Inductive Parametric Variations

In order to observe DUT behavior with inductive parametric variations, simulation conditions were as follows.

- $V_{\text{DD}} = 3.0$ V, $f = 735.29$ MHz, $T = 27^\circ$ C.
- $G$ changes from 1 to 300 using a logarithmic scale, that is, steps of 10 between 0 and 100 and steps of 100, between 100 and 300.
- For each value of $G$, $R$ changes between 1 and 5 $\Omega$ using steps of 1 $\Omega$.
- $L$ fixed at 10nH.

The achieved results were very different from the results achieved before. Now, the correct signature “30” was only obtained for $G=10$. For $G>10$, an erroneous output was obtained. Correct functionality requires $V_{\text{CUT}} > 2.88$ V and $I_{\text{CUT}} < 1.863$ mA.
6.3.2 Xtran.v2 as Pipeline Stage

The original Xtran.v2 circuit presented in Figure 59 was modified with the addition of a new FF between the cone output and the MISR as presented on Figure 68.

![Circuit Diagram](image)

*Figure 68- Xtran.v2 with a data capture register in a BIST environment.*

6.3.2.1 Original Circuit

For the Xtran.v2 pipeline DUT and $V_{SET-UP} = 3.0V$, $f_{max}$ yields 816.33 MHz (clock period of 1.225 ns) and the correct decimal signature value is “30”. This frequency result is similar to the result obtained with Xtran.v1. This results from the addition of the new flip-flop in the circuit. As described in 6.3.1.1, with this new element the circuit critical paths are different and so the circuit behavior. The value achieved for the combinational block, 666.66 MHz represents 81.66% of this new value.

For this pipeline Xtran.v2 DUT and with the proposed set-up circuit, new simulations were performed. The experimental conditions were as follows.

- $V_{DD} = 3.0V$, $f = 816.33 MHz$, $T = 27^\circ C$.
- G changes from 1 to 300 using a logarithmic scale, that is, steps of 10 between 0 and 100 and steps of 100, between 100 and 300.
- For each value of G, R changes between 1 and 5 $\Omega$ using steps of 1 $\Omega$.

Under these conditions, no correct behavior is obtained. For $G = 0.1$, circuit responses are correct as shown in Figure 69.
6.3.2.2 Modified Circuit (with DDB Insertion)

For Xtran.v1 as a pipeline circuit and recurring to the DyDA tool, a solution was achieved as specified in 6.3.1.1. For the Xtran.v2 the solution is the same, as the only difference between versions is a NOR gate instead of a NAND gate. Hence, the circuit critical path is the same for both versions and the DDB insertion is done in the same flip-flops as illustrated in Figure 70.

With this solution, a new maximum frequency was identified for a fixed $V_{DD} = 3.0$ V. The maximum value that still presents the correct signature “30” is 1015.8 MHz ($\tau_0 = 0.98$ ns), an improvement of 19.6% as compared to the original circuit.

In order to compare the results achieved to the original circuit, simulations were performed with the same conditions. Results are shown in Figure 71. The correct signature was achieved for the all resistance values combined with $G \in (10, 30)$. From $G=40$ until $G=90$ only some of the resistance values yield the correct signature. For $G=100$, only $R=1 \Omega$ delivers the correct value, just like the results presented for Xtran.v1 as a pipeline circuit with DDB. Correct functionality quests for $V_{CUT} > 2.79$ V and $I_{CUT} < 1.72$ mA.
6.3.2.3 Inductive Parametric Variations

In order to observe the CUT behavior with inductive parametric variations, simulation conditions are as follows:

- $V_{DD} = 3.0\, \text{V}$, $f = 816.33\, \text{MHz}$, $T = 27^\circ\, \text{C}$.
- $G$ changes from 1 to 300 using a logarithmic scale, that is, steps of 10 between 0 and 100 and steps of 100, between 100 and 300.
- For each value of $G$, $R$ changes between 1 and 5 $\Omega$ using steps of 1 $\Omega$.
- $L$ fixed at 10nH.

The achieved results were very different from the results achieved before. The correct signature “30” was only obtained with $G=10$. For $G>10$, the circuit response wasn’t correct. Now, correct functionality requires $V_{\text{CUT}} > 2.89\, \text{V}$ and $I_{\text{CUT}} < 1.85\, \text{mA}$.

6.4. Delay Fault Detection (Bridging Faults)

6.4.1 – Xtran.v1

Fault injection was carried out assuming resistive bridging defects. The defect is modeled by a linear resistance $R_{cc}$, as shown for Xtran.v1 in Figure 72. The location of the resistive bridging fault is chosen in such a way that it may influence the critical path. As referred, the critical path for the fault-free Xtran.v1 and Xtran.v2 cones is the X6-G5-G6-Q path. Hence, by injecting a BRI fault between X3 and X4, as X4 and X6 are both inputs for the same gate, we hope to inject a fault that can be detected by delay testing. Circuit simulation proves such fault is detectable for the original and modified CUT, although for different $V_{DD}$ values and $R_{cc}$ values.
With the resistive bridging applied to Xtran.v1, new results were obtained. The simulation conditions were as follows.

- $V_{SET-UP}$ variable from 1.7 V to 3.3 V.
- $f = 735\text{MHz}$, $T = 27^\circ \text{C}$.
- $R_{cc}$ variable from 0 to 60 kΩ, with an increment of 10 kΩ, and then fixed at 100 MΩ.

For the original circuit, with BRI fault injection ($R_{cc}$ between X3 and X4), the set of signatures is presented in Figure 73. Hard shorts correspond to $R_{cc}=0$ Ω. For $R_{cc}=10k\Omega$ and $V_{DD}=3.0V$, the fault is also detected, as the (faulty) circuit signature is not “93” as expected.

For the other $R_{cc}$ values the circuit behavior is as expected, presenting the correct value for a $V_{DD}>3.0V$.

For the modified circuit, the DDB cell was applied to the circuit as specified in 6.1.3.2. As it can be seen circuit correct respond, signature "93", is achieved for the $R_{cc}$ values from 100 MΩ to 10 kΩ with $V_{DD}$
assuming values from 3.3V to 2.6V. For \( R_{cc} = 0 \Omega \), (short-cut) the fault is detected for all \( V_{DD} \) values, once the circuit response is different from as showed in Figure 74.

![Figure 74- Set of signatures of the modified Xtran.v1 with a resistive bridging (variable \( V_{DD} \), \( R_{cc} \)).](image)

6.4.2 - Xtran.v2

Fault injection was carried out assuming resistive bridging defects. The defect is modeled by a linear resistance \( R_{cc} \), as shown for Xtran.v2 (see Figure 75).

![Figure 75- Resistive bridging applied to Xtran.v2 circuit.](image)

With the resistive BRI fault applied to Xtran.v2, new results were achieved. The simulation conditions were as follows.

- \( V_{SET-UP} \) variable from 1.7 V to 3.3 V.
- \( f = 666.66 \text{ MHz} \), \( T = 27^\circ \text{C} \).
- \( R_{cc} \) variable from 0 to 60 k\( \Omega \), with a increment of 10 k\( \Omega \), and then fixed at 100 M\( \Omega \).

For the original circuit, the set of signatures obtained with the introduction of \( R_{cc} \) between X3 and X4 is presented in Figure 76. As it can be seen, the BRI fault is detected when \( R_{cc} = 0 \Omega \) (shortcut), as the circuit signature is not “92” as expected.
Figure 76- Set of signatures of the original Xtran.v1 with a resistive bridging (variable V_{dd}, R_{cc}).

For the modified circuit, the DDB cell was applied to the circuit as specified in 6.3.2.2. As it can be seen in Figure 77 circuit correct signature "92", is obtained for R_{cc} values from 100 MΩ to 10 kΩ with V_{dd} ∈ (2.6; 3.3)V. For R_{cc}=0 Ω (short-circuit between X3 and X4) the fault is detected for all V_{dd} values. The introduction of a DDB cell in the circuit enhances tolerance to V_{dd} variations. Hence, the BRI fault is detected for lower values of V_{dd}, as compared to the original circuit.

Figure 77- Set of signatures of the modified Xtran.v2 with a resistive bridging (variable V_{dd}, R_{cc}).

6.4.3 Xtran1 as Pipeline Stage

As for the previous CUT, a bridging fault was injected (in the same location, between X3 and X4) in the pipeline environment, in order to compare results.
With the resistive bridging applied to Xtran.v1 pipeline stage, new simulations were run, under the following conditions:

- $V_{SET-UP}$ variable from 1.7 $V$ to 3.3 $V$.
- $f = 813$ MHz, $T = 27^\circ$ C.
- $R_{cc}$ variable from 0 to 60 k$\Omega$, with an increment of 10 k$\Omega$, and then fixed at 100 M$\Omega$.

For the original circuit, the set of signatures with the introductions of $R_{cc}$ is presented in Figure 78. As shown, the BRI fault is detected for the short-circuit situation ($R_{cc}=0$ $\Omega$) independently of the $V_{DD}$ voltage. This result is easily identified, as the correct decimal signature, “30”, is obtained for all $R_{cc}$ values, except $R_{cc}=0$ $\Omega$ for $V_{SET-UP} > 3.0$ $V$.

For the two-clock (modified) circuit, results are shown in Figure 79. As expected, the fault is detected for $R_{cc}=0$ $\Omega$. For the other values of $R_{cc}$ the fault is not detected. This can be seen by the set of correct signature “30” achieved for a $V_{DD}$ value upper then 2.5V.

![Figure 78](image1)

**Figure 78-** Set of signatures of Xtran.v1 pipeline stage original circuit with $R_{cc}$ between X3 and X4.

![Figure 79](image2)

**Figure 79-** Set of signatures of Xtran.v1 pipeline stage modified circuit with $R_{cc}$ between X3 and X4.
6.4.4 Xtran2 as Pipeline Stage

For the Xtran.v2 circuit, a set of similar experiments was performed. Simulation conditions were as follows.

- V\textsubscript{SET-UP} variable from 1.7 V to 3.3 V.
- f = 816.33 MHz, T = 27º C.
- R\textsubscript{cc} variable from 0 to 60 kΩ, with a increment of 10 kΩ, and then fixed at 100 MΩ.

For the original circuit, again the BRI fault is detected for the shortcut situation R\textsubscript{cc}=0Ω. For V\textsubscript{DD} > 3.0V, the correct signature is obtained for all R\textsubscript{cc} values (in Figure 80).

![Figure 80- Set of signatures of Xtran.v2 pipeline stage original circuit with R\textsubscript{cc} between X3 and X4.](image)

For the modified circuit the response is as expected, the fault is also detected for the short-circuit situation. The difference for the original circuit is the fact that the correct signature is obtained for higher V\textsubscript{DD} values, being correct for V\textsubscript{DD} > 2.5V (Figure 81).

![Figure 81- Set of signatures of Xtran.v2 pipeline stage two-phase clock circuit with R\textsubscript{cc} between X3 and X4](image)
6.4.5 Special Cases

A new set of experiments was performed, using a limited subset of the search space. We consider \( L = 10 \, \text{nH} \) and the corresponding upper \((G, R)\) values for which correct functionality is obtained, in fault-free CUT. We refer it as \((G, R)_{\text{max}}\). All analyzed circuits are in the modified versions (with DDB insertion), as for \( V_{\text{DD}} = 3.0 \, \text{V} \) all original versions failed to present the correct signatures. The objective is to analyze delay fault detection, for the same resistive BRI fault considered in previous simulations.

6.4.5.1 Xtran.v1 \((G, R, L, \text{Rcc})\)

As referred in 6.1.3.3 for \( L = 10 \, \text{nH}, \) \((G, R)_{\text{max}} = (100, 4 \, \Omega)\). With these constraints and applying the simulation conditions described in 6.4.1 experiments were performed. Results show that the BRI fault was detected for all \( V_{\text{DD}} \) and \( \text{Rcc} \) values. The source of the problem is that, by introducing so much power noise, \( V_{\text{CUTave}} \) decreases down to 2.7V. Hence, as compared to the results presented in 6.4.1, \( V_{\text{CUTave}} \) is almost the same. In this case, circuit failure occurs prematurely.

This is a reduction of 100% in the circuit correct behavior if we compare to the results achieved in 6.4.2. With the introduction of \((G, R, L)\), \( V_{\text{CUTave}} \) in the presence of \( \text{Rcc} \) has decreased from 3.3V to 2.6V which leads to a \( V_{\text{CUT}} \) reduction of 19%.

6.4.5.2 Xtran.v2 \((G, R, L, \text{Rcc})\)

For the Xtran.v2 the same procedure was performed. Now, \((G, R)_{\text{max}} = (100, 2 \, \Omega)\). With these constrains, circuit response to \( \text{Rcc} \) injection was more tolerant than before. In fact, the BRI fault was identified for all the \( \text{Rcc} \) values; however fault detection occurs for different \( V_{\text{DD}} \) values. The circuit’s correct functionality was obtained with \( V_{\text{DD}} = 3.3 \, \text{V} \) and with all \( \text{Rcc} \) values except for \( \text{Rcc} = 0 \, \Omega \). For all other variations, circuit behavior wasn’t the correct one. The correct signature was achieved for \( V_{\text{CUTave}} > 2.6 \, \text{V} \). Hence, in comparison to the results presented in 6.4.2, \( V_{\text{CUTave}} \) is the same, only in this case it is achieved in the first place.

This is a reduction of 75% in the circuit correct behavior if we compare to the results achieved in 6.4.2. With the introduction of \((G, R, L)\), the \( V_{\text{CUTave}} \) in the presence of \( \text{Rcc} \) has decreased from 3.3V to 2.6V (a 21% reduction).

6.5. Voltage and Temperature Variations

Finally, the temperature parameter was introduced in the experiments, together with \( V_{\text{DD}} \) variations. Here, only simulation results for Xtran.v1 are shown, for a single pair of \((G, R)\) values. The circuit was tested under the following conditions:

- Frequency fixed at \( f = 735 \, \text{MHz} \).
- \( R = 5 \, \Omega, G = 40 \) in the first simulation, and \( G = 50 \) in the second simulation.
- Temperature changing from 27° to 147° C with steps of 20° C.
- \( V_{\text{DD}} \) voltage changing from 2 V to 3.3 V with steps of 0.1 V.
With these conditions, the results for the original Xtran.v1 CUT in the BIST environment (illustrated in Figure 49) are shown in Figure 82. As it can be seen, no \((V_{DD}, T)\) pair of values leads to a correct signature value.

In the modified circuit (with the introduction of a DDB cell as depicted in Figure 51), correct results are obtained for different values of \(T\), as shown in Figure 83.

It is possible to observe that the correct signature “93” is obtained for \(V_{DD} \in (3.2, 3.3)\) V and temperatures between 27°C and 67°C. For lower values of \(V_{DD}\), like 3.1 V, a correct signature is obtained until \(T=47°C\). For \(V_{DD}\) values of 3.0 V and 2.9 V, only at the lowest temperature (\(T=27°C\)) the correct functionality is observed. Hence, the insertion of a DDB cell in the circuit has made the circuit more tolerant to temperature and voltage variations.
For the $G = 50$, and with the original Xtran.v1 circuit, none of the $(V_{DD}, T)$ combinations produced the correct signature value, as shown in Figure 84.

![Figure 84- Set of signatures achieved for $G=50$ $R=5\ \Omega$ and with $V_{DD}$ and Temperature variations.](image)

With the insertion of a DDB cell, results are more interesting. For the simulation conditions described in 6.1.2, the circuit couldn’t present the correct signature for the combination $G=50$, $R=5\ \Omega$ once the power supply voltage was fixed at 2.97 V. However, these additional simulations show that with a minor difference of 0.03V, the correct signature is obtained for the $(50, 5\ \Omega)$ combination. The results are shown in Figure 85. For these $(G, R)$ combinations, the correct signature is obtained for $V_{DD}=3.3\ V$ and $T < 67^\circ\ C$. For $V_{DD}=3.2\ V$, only for temperatures bellow 47° C the circuit operates correctly. For $V_{DD} \in (3.0, 3.3)\ V$, only for $T= 27^\circ\ C$ a correct signature is obtained. Again, with these results it is possible to confirm the added tolerance introduced by the DDB architecture.

![Figure 85- Set of signatures achieved for $G=50$ $R=5\ \Omega$ and with $V_{DD}$ and Temperature variations with DDB.](image)
7. Conclusions and Future Work

7.1. Conclusions

As referred, the objective of the work was to analyze the effectiveness (and limitations) of the VT-aware methodology in the presence of non-ideal power supply voltages namely in a DfT environment, using BIST or scan design techniques.

A methodology to experiment the VT-aware design methodology under non-ideal $V_{DD}$, in digital circuits with DfT, in normal and test modes, was proposed in chapter 3. A lumped set-up circuit has been introduced, and thoroughly used. The set-up circuit has only two model parameters (the gain factor, $G$, and the unit resistance of the metal power supply lines, $R$), to emulate digital circuit complexity, and local power grid non-ideality.

A set of combinational, pipeline and sequential circuits has been used as test vehicles. Xtran industrial module, Xtran.v1 and Xtran.v2 blocks, as well as the B06 ITC’99 benchmark circuit, have been selected to cover the set of relevant situations. A target IC technology and cell library (AMS 350 nm CMOS) was used to implement all examples. TPG and TAE have been used to emulate self-test conditions under pseudo-random test generation (LFSR, MISR). Scan design is also used in the sequential B06 circuit.

Digital circuit timing response in presence of power supply noise (PSN) has been extensively analyzed. It was demonstrated by simulation that the VT-aware design methodology holds in the presence of PSN, and of test circuitry associated to the use of DfT techniques, like BIST and scan, both in normal and test modes of operation.

In terms of PSN, a relevant conclusion is that the impact of non-ideal $V_{DD}$ voltage source on the timing response leads to a decrease on the average voltage applied to the CUT ($V_{CUTave}$) and to the presence of a ripple component, $v_{cut}(t)$. When compared with results from ideal $V_{DD}$ sources of variable (DC) values, time responses are mainly modulated by $V_{CUTave}$ being relatively insensitive to $v_{cut}(t)$. This is reasonable, since the noise margins of the CMOS gates are enough to allow a clear discrimination between the two logic states, 0 or 1. Of course, this conclusion holds for ripple components which do not compromise the correct functionality (peak $v_{cut}$ value lower than $V_{DD}/2$). In terms of non-ideality, observation is that IR drop effects are more relevant than L effects. Moreover, circuit complexity (described, in the proposed set-up circuit by the gain fact, $G$), for a given non ideality ($R$, $L$ values) exhibits a similar pattern. Again, as complexity increases and $V_{CUTave}$ decreases, the time response is degraded in a similar fashion. Therefore, regardless of the root cause ($V_{DD}$ non-ideality and/or circuit complexity), the designer may estimate $V_{CUTave}$ and predict the overhead in propagation delays, thus acting to enable time borrowing, increasing circuit tolerance. This can be a useful circuit design guideline. As an example, for the Xtran.v1 circuit and manual DDB insertion, the maximum tolerance can be obtained with the following parameter pair values: $(G, R) = (200, 1\Omega), (100, 2\Omega), (50, 4\Omega), \text{and} (40, 5\Omega)$. It is possible to identify a merit factor, which is the product (G.R); in this case, with variable $G$ and $R$, G.R=200$\Omega$ for all cases. This does not mean that we get always a constant G.R value. For instance, for the same example and with DDB insertion suggested by DyDA, the results were: $(G, R) = (300, 1\Omega), (200, 2\Omega), (100, 4\Omega), \text{and} (50, 5\Omega)$. However, these results clearly show the impact of $V_{CUTave}$ on VT tolerance.
In all simulated cases, a significant improvement (in the order of 15-20%) in circuit tolerance to VT variations for all the tested circuits has been observed.

In limited way, it was demonstrated in this dissertation that the dynamic time borrowing concept, associated to DDB insertion, can be applied in DfT circuits, in normal and test mode, leading to enhanced tolerance to VT variations, while still allowing delay fault detection in a multi-\( V_{DD} \) test (or self-test) environment. Scan design was shown in the B06 sequential benchmark. BIST environment was shown for the Xtran industrial design. As far as normal and test modes of operation, DyDA suggests DDB insertion, regardless of the operation mode. Hence, in both modes a correct timing behavior is enlarged, due to time borrowing. A very interesting aspect that has been highlighted is that critical paths may be identified in the functional circuit, and/or in the test circuitry. If a multi-\( V_{DD} \) test environment is envisaged, for at-speed delay fault detection, the test circuitry must be designed to operate correctly for a wide range of \( V_{DD} \) values, as we do not want the circuit to fail the test, due to a failure in the test circuitry. Delay fault detection was verified, using a multi-\( V_{DD} \) test environment, for resistive bridging faults disturbing the critical paths. Fault detection, using the VT-aware methodology, occurs (of course) for lower \( V_{DD} \) values, due to time borrowing. The range of \( R_{cc} \) values for which fault detection occurs is modified, according to the new range of \( V_{DD} \) values.

Finally, circuit-level simulation ascertained that the proprietary software tool, DyDA, is effective in identifying (with PrimeTime™) the circuit critical paths, defining maximum frequency of operation and proposing the number and location of DDB cells to be inserted. Cells may be inserted either in the clock signal path of some registers (CME), or in the signal path of some short delay paths in the data path. Manual and automatic DDB insertion (as proposed by DyDA) has been tested, and the superiority of the DyDA solutions was proven e.g., in the Xtran.v1 in BIST environment have presented 40% of improvement with automatic DDB insertion.

### 7.2. Future Work

In this dissertation, two key issues are addressed. First, we investigate the effects of non-ideal \( V_{DD} \) sources, due to non-ideal power grids in digital systems, on circuit performance. Second, we show that it is possible to implement the VT-aware methodology in digital circuits designed with DfT, for variable complexity and non-ideal \( V_{DD} \). The demonstration was performed within given constraints. Further work is easily foreseen in the following areas:

- The effect of process variations was not addressed in this work. It can be considered, provided that technology information is available.
- A more aggressive IC technology (namely, 65 or 45 nm) should be used to ascertain the results. As stated, this IC technology was used, as it was available.
- Use of adequate test sequences, generated by an ATPG for delay faults (transition and path delay faults associated with the critical paths, identified by PrimeTime), in order to test the combinational, pipeline and sequential circuits in situations for which time borrowing can more completely be examined. Such deterministic test patterns may easily be applied in non-BIST environments. Deterministic BIST is a more complex process.
In terms of pipeline circuits, only single-stage pipeline (Xtran, Xtan.v1 and v2) circuits were tested. Multi-stage pipeline circuits testing should be performed, in order to guarantee that the amount of borrowed time can be recovered in subsequent stages.

In terms of scan design, DfT techniques for delay testing consider LOC (Launch on Capture) or LOS (Launch on Shift) techniques [16]. Such solutions should also be tested, in order to see how well the VT-aware design methodology holds.

Logic-level and circuit-level results of time performance, for a given IC technology and cell library, are similar, but not equal. After IC physical design, layout extracted parasitics can fine-tune the node capacitances, which also impact timing. We verified that PrimeTime™ provides conservative estimates of $f_{\text{max}}$. Moreover, DyDA defines which critical paths are selected for DDB possible insertion, using logic-level timing information. A more thorough verification if gate-level results can reliably be used for CP selection may be needed; otherwise, some CP can emerge in the final circuit, which was not considered by the methodology. This is more a refinement of the VT-aware methodology, out of the scope of this dissertation. However, it was this work that draws our attention for this question.
References


[35] www.cadence.com
[36] www.synopsys.com


Complete overview of Xtran.