Experimental Validation and Performance Analysis of the Clear-PEM Data Acquisition Electronics

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Abstract: Obtaining images with high resolution and contrast from short exams is crucial for the viability of Positron Emission Mammography as an early breast cancer detection technique. The Clear-PEM detector is a Positron Emission Mammography scanner, developed by the Portuguese Consortium in the framework of the Crystal Clear Collaboration at CERN, based on high-granularity avalanche photodiodes readout with 12288 channels, coupled to pixilated 2x2x20 mm³ LYSO:Ce crystals in a double readout configuration. The scanner features a high bandwidth three-level acquisition system with negligible dead time in order to minimize exam time. The frontend is instrumented with low-noise amplifier/discriminator/multiplexer ASICs (L0 trigger) and free-running ADCs while the off-detector electronics, implemented in FPGAs, computes the trigger primitives from the pulse amplitude and timing. With this information the readout electronics selects interesting photoelectric events and groups multi-hit events due to in-Compton scatter into possible coincidences. After a first-level trigger (L1) is generated, filtered data is read out over a high speed data link into a second-level (L2) software trigger which reprocesses the selected events in temporal coincidence with more accurate energy and time extraction algorithms. The DOI coordinate and the re-validated energy and time allow to achieve an improved reconstruction of in-detector Compton scattering and rejection of random and scattered coincidences. On this paper, we report on the experimental validation, characterization and optimization of the L1 data acquisition electronics, readout link and L2 software trigger and present performance results. We discuss the validation of the associated operation software.

1. Introduction

Using Positron Emission Mammography for breast cancer tracing, requires the ability of producing high resolution images from short exams. The Clear-PEM detector is a planar prototype system designed for imaging the breast and axilla, based on pixilated LYSO:Ce scintillator crystals read out on both ends by avalanche photo-diodes (APD). To achieve the necessary system detection sensitivity and spatial resolution, the Clear-PEM detector features a high performance data acquisition system that exploits on-line computation of time and event to select at an early stage candidate two photon events in coincidence, depth-of-interaction (DOI) coordinate determination and reconstruction of Compton scattering in the detector. The system implements individual energy, time and DOI channel calibration. To conciliate the large number of readout channels (12²288), the high event rates (up to 5 MHz of single photons in each detector head) and the need for sophisticated event processing the data acquisition system employs multi-level data selection and trigger architecture capable of sustaining a high event rate with negligible dead time. The Clear-PEM electronics and computing infrastructure (frontend ASIC, L1 electronics acquisition crate, L2 software) were developed in parallel over a time span of 3 years. Before these major blocks could be fully connected, methodologies were developed in order to perform most of the electronics verification and validation, well in forehand of the final detector integration. In this paper the hardware that mimics the frontend readout electronics used to validate, characterize and optimize the L1, L2 trigger levels and operation software of the Clear-PEM acquisition system is described as well as the main experimental results. Commissioning of the Clear-PEM frontend electronics, namely the detector supermodules, each one including 384 LYSO:Ce crystals, 24 S8550-01 APD matrices from Hamamatsu and 4 readout ASIC is undergoing tests. Results on the characterization of the supermodules will be presented at this conference in a separate paper [1].

2. Overview of the Clear-PEM Data Acquisition Electronics

Low-noise integrated electronics mechanically fixed and electrically connected to the detector modules provides signal amplification and analog multiplexing for a total of 12²288 APD output channels. The Clear-PEM frontend ASIC integrates 192 channels and selects one or two channels above a common threshold. The analogue samples are digitized
in the frontend by 10-bit sampling ADCs running at 50-100 MHz, which provide the input digital data streams to the first trigger level and data acquisition electronics, housed in a off-detector 6U crate with two CompactPCI backplanes. Up to 156 Gbps of data are continuously transmitted from the frontend to the off-detector L1 electronics which selects events up to a maximum of 6.4 Gbps. Two types of electronic boards were developed, namely the Data Acquisition Boards (DAQ Boards) and the Trigger and Data Concentrator Board (TGR/DCC Board) equipped with 4 and 3 million gates Xilinx Virtex II FPGAs. DAQ Boards performs the initial phase of data reduction/selection (pipeline data storage, parallel algorithmic processing to extract the amplitude and time of the detector hits) and transmit the potentially interesting events to the TGR/DCC board which performs the trigger candidate selection. Selected possible coincidences’ data, composed of channel identifiers, digital samples and time tags are transmitted to a computer over a high speed data link. For the data link between the L1 and L2 trigger, a solution named FEDKit [2] was adopted. This link is an SLINK-64 implementation developed for the Compact Muon Solenoid (CMS) experiment at CERN and is capable of transmitting up to 800 MB/s aggregate bandwidth at a 100 MHz clock frequency input. Data is carried over in 64-bit words. The FEDKit link consists of a transmitter CMC mezzanine card installed on the L1 crate and a receiver CMC mezzanine card mounted to a 64 bit, 66 MHz PCI-X card on the L2 Trigger Acquisition Computer. The L2 trigger stores the received data on a SAS disk array capable of sustaining transfer rates up to 420 MB/s while, in parallel, it reprocesses the received data using more accurate algorithms than those implemented in the L1 trigger electronics. The more accurate algorithms allow an improved rejection of random and scattered coincidences and a more accurate accounting of Compton scattering in the detector. Along with event reconstruction the operating software collects statistics of the detected events, such as energy spectrum, pedestals per ASIC channel, noise per ASIC channel, which are used to monitor the performance of the detector and locate any problems such as dead or noisy channels. The Visualization Computer runs a Graphical User Interface (GUI) that controls the software in the L2 Trigger Acquisition Computer and provides the user with access to the collected statistics.

2.1 Performance of L1 Data Acquisition and Trigger Electronics

Not actually a part of the Clear-PEM detector, the Front-End Emulators (FE-EMU) are custom VME64 modules that mimic the output of the Clear-PEM frontend electronics using programmable patterns obtained from Monte Carlo simulations. These are used to validate and test the downstream components (L1 and L2) of the Clear-PEM acquisition system by transmitting known data, at rates ranging from 100 Hz to 2.4 MHz (2.4 million events/s). The system was monitored at two points: the coincidence trigger (TGR) and the output data concentrator (DCC) implemented in the FPGA of the TGR/DCC board. As shown in Fig. 1a, the coincidence trigger scales linearly with the input event rate, up to 2.4 MHz, and no data is lost. This result confirms the excellent behavior of the L1 firmware, already foreseen in detailed simulations. The event rate at the output data concentrator scales linearly with the input rate up to 800 kHz as can be observed in Fig. 1b. Above 800 kHz, limitations on the current version of the firmware and bandwidth occupation in the inter-card buses start to be responsible for the introduction of dead-time, asymptotically decreasing the readout rate to the L1-L2 data link down to 500 kHz. An improved firmware version should allow to coincidence rates up to 1 MHz without significant loss of efficiency.

2.2 Performance of L1-L2 FEDKit Data Readout

Testing of the FEDKit readout data link was performed by transmitting test patterns in blocks of diverse sizes, from 8B to 128KiB bytes - Fig. 1c. The link input clock was set to 66 MHz which means that a maximum transfer of 66 MHz x 64 bits = 520 MB/s can be achieved. In this work we have ported the FEDKit driver delivered to us by CMS, designed to be used with a Linux kernel 2.6, 32 bit to a 64 bit version as required for our application. Results show that the system's efficiency increases with block size reaching a maximum transfer rate of 517MB/s for 128KiB blocks, near the theoretical maximum of 520MB/s. A size of 32KiB block size was selected for further testing as a compromise of high link efficiency (509 MB/s) and small buffers on the L1. The readout data link was also tested for the (BER) bit error rate. The tests were stopped after 60 TiB of test patterns were transmitted without errors since it guaranteed a sufficiently low BER (< 10⁻¹⁵). The system's capability of receiving data from the data link and writing it to disk was also assessed, as is shown in Fig.1d. It was found that while the disk array could sustain data rates of 420MB/s. A decrease as function of the data transferred increases was observed due to the file system's performance being degraded as the SAS array fills up. Nevertheless, the minimum sustain data transfer of 300MB/s for a full file system is more than enough for the data transfer requirements. In standard breast/axilla exam the expected L1 trigger rate is of about 50-150 kHz or 15 MB/s. In detector normalization scans, the most demanding operation mode for the scanner, the L1 trigger rate can top 1 MHz, generating about 200 MB/s.
2.3 Performance of L2 Trigger and Operation Software

The operation software designed to control the Clear-PEM scanner exploits the intrinsic independence of the events to parallelize the workload. Tests carried out in the L2 trigger system, equipped with two 3.2GHz dual core CPUs, have shown that the system was able to reprocess and collect statistics at a rate of 1 million events per second. The L2 reconstruction rate is mainly limited by the decoding of received data which has not been parallelized. The software validation process includes unit and regression tests as well as simulated acquisitions. For the simulated acquisitions we replace the FEDKit driver module with a dummy driver that reads previously acquired data files while generating errors on occasion. Although deterministic tests allow many problems to be detected, we found that it can't accurately model the response of the L1 electronics to stochastic events and thus, the ability to validate the system using the FE-EMUs is invaluable.

3. On-Going and Future Work

A second phase of the characterization of the L1 Trigger electronics using the described FE-EMU test crate will be performed in order to test a new firmware that will allow a deadtimeless readout up to 1 MHz event rate. The Clear-PEM scanner is now on its final integration phase. With the start of the commissioning phase new characterization tests of the performance of the system will be performed and results will be presented at this Conference.

References:
