Comparing the Efficiency of a Clock-Signal Modulation Technique for System-on-Chip in Conducted Versus Radiated EMI Environments


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Abstract
This paper1 compares the effectiveness of a Clock Duty-Cycle (CDC) Modulation technique to enhance System-on-Chip (SoC) signal integrity with respect to two different disturbance sources: power-supply voltage transients and radiated electromagnetic interference (EMI). This technique dynamically adapts the CDC according to signal propagation delay through the logic whose power supply voltage is under disruption. The technique is based on a clock stretching logic (CSL) block, which monitors abnormal power grid activity and increases CDC accordingly. Practical experiments based on a 32-bit soft-core pipeline processor implemented with the proposed technique in a FPGA IC were performed. The obtained results analyze and compare the CDC Modulation technique efficiency in conducted versus radiated EMI environments. These experiments were based on the IEC 61.004-29 and 62.132-2 standards for conducted and radiated EM immunity measurements.

1. INTRODUCTION
Signal integrity is the ability of a signal to generate correct responses in a circuit. It generally includes all effects that cause a circuit malfunction due to the distortion of the signal waveform [1,2]. According to this definition, a signal with good integrity presents: (i) voltage values at required levels and (ii) level transitions at required times. For instance, an input signal to a flip-flop with good signal integrity arrives early enough to guarantee the setup and hold times and it does not have spikes that may cause undesired logic transitions [3,4].

In this scenario, the underlying principle of the presented methodology is to dynamically adapt the CDC according to the signal propagation delay through the logic whose power supply voltage is being disturbed [5]. The functionality to implement this principle is as follows: (1) power supply voltage monitoring and (2) when voltage variation exceeds a user’s defined threshold, CDC modulation. Hence, the correspondent architecture contains a clock stretching logic (CSL) block, to monitor power grid activity (VDQ undershoots and/or ground overshoots) and to enhance the clock duty-cycle provided by the phase-locked loop (PLL) block to the controlled logic when required.

The main advantage of the proposed methodology is to render the circuit more robust to power line fluctuations by maintaining at-speed clock rate. As such fluctuations are often due to circuit operation, they tend to cause local disturbances in the power grid. Hence, it is a waste to reduce the clock frequency in the overall system. The proposed methodology locally adapts the CDC without loosing circuit performance.

In this work, we are concerned with analyzing and comparing the effectiveness of the Clock Duty-Cycle (CDC) Modulation technique [6] to enhance SoC signal integrity with respect to two types of EMI: conducted and radiated. Practical experiments based on the implementation of a 32-bit soft-core pipeline processor according to the proposed technique in a FPGA IC were performed and compare the processor robustness enhancement to EMI in both cases, while maintaining at-speed IC clock rate.

2. THE CDC MODULATION METHODOLOGY
The proposed methodology is based on the following assumptions (see [5] for a complete description):

a) CDC is generally set at 50% to minimize the jitter effect and uncertainties associated with parameters spread due to process variations; and to allow a weighted-time distribution for circuits designed with both rise- and fall-edge triggered flip-flops.

b) The maximum value to which CDC can be stretched is significantly lower than 100% (otherwise, the combinational logic part collapses). In practice, the maximum allowed value is 80%.

c) CDC may be temporarily modified for some functional parts of a SoC, but maintained unchanged for the other parts. This does not result in circuit functional error if the overall clock rate is kept unchanged and all the combinational parts of the circuit keep working at-speed IC clock rate.

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1 This work has been partially funded by CNPq (Science and Technology Foundation, Brazil).
Consider a synchronous IP core with different modules, each fed by a subsection of the power grid infrastructure (Fig. 1). If circuit operation induces $V_{DD}$ variations in module $i$, its timing performance is distorted, typically delayed. In order to allow the combinational blocks to correctly finish their job, an additional time has to be given to the signals switching in critical paths. Hence, the underlying idea is to dynamically delay their capture by the critical memory elements at the end of critical paths, in the presence of $V_{DD}$ variation. Therefore, for a limited subset of the module’s registers ($m < k$), a CDC modulation block must be added to accommodate such delay.

In a synchronous circuit, CDC is generally set at 50% to minimize jitter and process variations, and to allow a weighted-time distribution for circuits designed with both rise- and fall-edge triggered flip-flops (FF). In order to prevent logic errors, we assume that CDC may be stretched up to 80%.

We refer to as CDCM (or CDC Modulation) module the one that implements this added functionality. Locally, the CDCM module monitors $V_{DD}$ variations and triggers CDC variations accordingly. For each IP module, static timing analysis is used to identify the critical paths, allowing us to determine how many CDC modulators should be inserted (and where). Here, we illustrate the methodology using one power grid partition, one functional module and one CDCM system.

As shown in Fig. 2a, the proposed CDCM architecture is based on a clock stretching logic (CSL) block, which monitors power grid activity and enhances the clock signal (CLK) delivered by the phase-locked loop (PLL) block to the controlled logic accordingly. In this architecture, the CDCM module performs disturbance monitoring and CDC stretching using a simple circuit and introducing a limited clock delay, $\tau_{o}$ (referred to as the intrinsic CDCM delay). During normal operation (nominal $V_{DD}$), the CSL delivers a modulated clock signal ($CLK_{CDCM}$) with a CDC around 50%. When $V_{DD}$ decreases, the CSL block stretches CDC according to $V_{DD}$ reduction. In this case, the time slack ($t_{PM}$) is increased by an amount $\tau_{o}$, i.e., $t_{PM} = t_{PM} + \tau_{o}(V_{DD})$. When the $V_{DD}$ voltage transient fades away, the CSL block starts gradually reestablishing the original clock duty-cycle (50%) to the controlled logic ($m$ Critical Memory Cells). Fig. 2b illustrates the two possible ways of stretching the CDC (delaying the rising edge or delaying the falling edge) depending on the type of the critical memory cells used.

![Fig. 2. (a) Basic architecture of the CDCM system; (b) Forms of stretching the CDC: delaying the rising edge of the clock cycle for rising-edge triggered Flip-Flops, or delaying the falling edge for falling-edge triggered Flip-Flops.](image)

### 3. EXPERIMENTAL RESULTS

Practical experiments [7,8] were performed on a 32-bit microprocessor, which was mapped into a FPGA IC. With this purpose, two versions of the processor were downloaded into two separated FPGAs mounted on an EMI-oriented test board. Aiming at analyzing and comparing the CDC Modulation technique effectiveness with respect to conducted and radiated EMI, these experiments are described hereafter.

The selected device was “Plasma”, a soft-core microprocessor which was retrieved from the Internet public domain “Opencores” (www.opencores.org). This is a 32-bit three-stage pipeline processor described in VHDL and mapped into a test board previously designed and implemented by the authors. Fig. 3 depicts the Plasma general architecture and its VHDL basic blocks. The processor was downloaded into the test board shown in Fig. 4. This is a six-layer board designed and fabricated in partial compliance with the standard IEC 62.132 for radiated and conducted electromagnetic (EM) immunity measurements (www.iec.ch).

The devices under test: 2 FPGAs (Xilinx Spartan 500E), 4 SRAMs, 2 Flashes and the 8051 microcontroller (including the Plasma processor mapped into these FPGAs) are placed on the so called “test side” of the board (Fig. 4a). This side contains also the ground layer of the board. The remaining control logic (a third FPGA, a second 8051 microcontroller, clock signal generators, reset-push bottoms, serial-communication connectors, and dedicated I/O pins for data monitoring and power-supply injection) are mounted on the “other side” of the test board (Fig. 4b). This board side also lays down the
VDD distribution network for the system. The four board inner layers are used for signal routing.

![Block diagram of the system](image)

Fig. 3. General architecture of the soft-core Plasma processor.

Among the facilities available in this board, there is a temperature sensor that allows us to perform a burn-in test in conjunction with IEC test sessions (www.iec.ch). Additionally, the devices on the “test side” have separated power-supply bus. This infra-structure allows us to individually control the voltage level provided to the VDD (resp. Gnd) bus of each of these ICs. Similarly, we can also perform individual RF-conducted noise injection into any of these ICs or combination of them through these dedicated power busses on the “test side”. To do so, a dedicated board (not shown in Fig. 4) containing special connectors for RF-conducted noise injection is attached on the periphery pins of the board shown in Fig. 4b.

Two versions of the Plasma processor were implemented and mapped into the FPGAs of the “test side”. The first version (namely, “Original”) had the CDC fixed to 50% during the whole experiment. In the second version (“CDC-Modulation”), the clock signal feeding the Multiplier Block of the Plasma processor was controlled by the proposed technique. To do so, the VHDL code describing the Plasma was modified by adding an external pin to the processor (i.e., an additional FPGA input pin) so that we could control the CDC addressing the Multiplier Block. The remaining blocks of the processor had the CDC fixed to 50%. The CDC was modified in such a way that when the modulation was activated, the rising edge of the clock signal was delayed. The Original and the CDC-Modulation processor versions were prototyped into separate FPGAs on the “test side” of the board (Fig. 4a), so that the same tasks and input vectors were simultaneously applied to both processors running in parallel during the experiment.

Note that:

1. It was selected the Multiplier Block to have the CDC controlled because this block was the only one in the Plasma description (Fig. 3) that had explicit clock signal declaration in the VHDL code. For the Plasma remaining blocks, the clock signal was declared as asynchronous actions triggered after instruction decoding from the Control Part. So, if other processor blocks had to be controlled, it would be necessary to carry out complex changes in the VHDL code.

2. All the D flip-flops (D-FFs) in the Original VHDL code of the Multiplier Block were declared as the type “rising-edge D-FFs”. So, when the CSL block modulated the clock signal in the CDC-Modulation VHDL version, it actually reduced the CDC from 50% to 25%. This action was carried out by delaying the rising-edge of the clock signal. Thus, it delayed the D-FFs triggering instant. Fig. 5 depicts this situation.

The clock signal generators for the Original version and for the CDC-Modulated version were also described in VHDL and implemented in the third FPGA, mounted on the “other side” of the board (Fig. 4b).

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1 IEC 62.132, IEC 61.004-17 and IEC 61.004-29.
Fig. 5. Summary of the original and the stretched clock waveforms: Original clock (clk\textsubscript{50%}); Stretched clock activating rising-edge FFs (clk\textsubscript{25%}).

3.1. The Radiated EMI Experiment

Fig. 6 depicts the test environment where the experiment was carried out [8]. The measurements were performed on a Gigahertz Transverse Electromagnetic (GTEM) Cell, which was used to radiate EMI on the test board. For the test sessions, the board was placed into a shielding box to prevent the glue logic on the “other side” of the board from being affected by the radiated EMI. Note that the “test side” of the board is placed outwardly the shielding box, so that the devices under test are exposed to radiation. Next, the whole set (test board and shielding box) was placed inside the GTEM cell, where the experiment was performed (Fig. 6).

![Test environment showing GTEM Cell and test vehicle](image)

(a) General view; (b) and (c) Closer views detailing the test board connected to the shielding box (with the “test side” turned out) into the chamber.

The experiment is the result of a total time of system exposition to radiated EMI of approximated 40 hours. The test conditions ruled by (but not limited to) the IEC standard 62.132-2 were as follows:

a) EM field range: from 10 to 220V/m;
b) Measured frequency range: from 150 KHz to 3 GHz (extended IEC 62.132-2);
c) Signal Modulation Format: AM 80%.

Additionally, the power supply pins of the two FPGAs containing the Original and the CDC-Modulation versions were slightly reduced to render the ICs more sensitive to noise during the radiated EMI tests. This condition was obtained by reducing 33% the voltage level feeding the FPGAs' \(V_{DD}\) pins as follows:

- Core: from 1.2V (nominal) to 0.80V.
- Periphery 1: from 2.5V (nominal) to 1.67V.
- Periphery 2: from 3.3V (nominal) to 2.21V.

Note that this 33% reduction in the \(V_{DD}\) pins of the FPGA did not induce faults in the system during normal operation (in a radiation-free environment), but simply rendered it more sensitive to noise when exposed to radiated EMI.

![Test environment showing GTEM Cell and test vehicle](image)

Fig. 6. Test environment showing GTEM Cell and test vehicle. (a) General view; (b) and (c) Closer views detailing the test board connected to the shielding box (with the “test side” turned out) into the chamber.

Fig. 7 summarizes the measured output values for the processor. For this experiment, the processor executed (in a time-shared basis) three application tasks under the control of its native operating system: Multiplication Matrix (MM), Curve Fitting (CF) and Cryptography (CR). The experiment was arranged in such a way that the processor executed the three tasks with the same priority. This condition allocated 33% of the CPU time to run each of the tasks. A shown in Fig. 7a, the use of the CDC-Modulation technique reduced the processor exposition to faults by an average factor of 39.36% ([1992-1208]/[1992],100%) with respect to the Original Plasma version.

Moreover, the usage of the Multiplier Block by the tasks was intentionally made not equal: task CR was the one that used intensively this hardware resource (i.e., most of the time the processor was based on the Multiplier Block to execute the task). Next, the MM task was implemented in such a way to use it moderately. Finally, the CF was the application task that least used the Multiplier Block (i.e., most of the time the processor was based on any unhardened logic, except in the Multiplier Block, to execute the CF task).

As shown in Fig. 7b, the Multiplier Block usage condition was reflected in terms of CDC-Modulation effectiveness. This reasoning is explained as follows:

a) Assume that the contribution of the faults occurred during the execution of the CR task to the system failure (\(C_{CR}\)) is given by the number of faults that occurred during the execution of the CR task (\(F_{CR}\)) divided by the total number of faults observed in the system (\(F_{S}\)). Then, \(C_{CR}\) was reduced from 83.48% ([290/1992],100%) in the Original Plasma version to only 1.82% ([22/1208],100%) in the CDC-Modulation version.

b) On the opposed direction, the contribution of the faults occurring during the execution of the MM task to the system failure (\(C_{MM}\)), that is given by the number of faults that occurred during the execution of the MM task (\(F_{MM}\)) divided by the total number of faults observed in the system (\(F_{S}\)), was increased from 14.56% ([290/1992],100%) in the Original Plasma version to 71.44% ([863/1208],100%) in the CDC-Modulation version.

![Number of Detected Faults](image)

Fig. 7. Summary for the IEC 62.132-2-based experiment.

- **Summary of the Original and the Stretched Clock Waveforms:**
  - **Original Clock (clk\textsubscript{50%}):**
    - **Stretched Clock Activating Rising-Edge FFs (clk\textsubscript{25%}):**

- **3.1. The Radiated EMI Experiment:**
  - **Test Environment Showing GTEM Cell and Test Vehicle:**
    - **General View:**
    - **Closer Views Detailing the Test Board Connected to the Shielding Box:**

- **Test Conditions:**
  - **EM Field Range:**
  - **Frequency Range:**
  - **Signal Modulation Format:**

- **Additional Power Supply Pin Reduction:**
  - **Core:**
  - **Periphery 1:**
  - **Periphery 2:**

- **Fault Reduction:**
  - **Processors:**
    - **Multiplier Block Usage:**
      - **CR Task:**
      - **MM Task:**
      - **CF Task:**

- **Graphical Representation:**
  - **Number of Detected Faults**
  - **PLASMA Version (as a Function of the Application Type):**

- **Reasoning:**
  - **Assumption:**
  - **Fault Contribution:**
    - **CR Task:**
    - **MM Task:**
    - **CF Task:**
Finally, similar conclusion can be taken upon analyzing the contribution of the faults occurring during the execution of the CF task to the system failure (C_{CF}), that is given by the number of faults that occurred during the execution of the CF task (\#F_{CF}) divided by the total number of faults observed in the system (\#F). In this case, C_{CF} increased from 1.96% ([39/1992].100%) in the Original Plasma version to 26.74% ([323/1208].100%) in the CDC-Modulation version.

In summary, while C_{CR} was reduced by approximately 46 times (83.48%/1.82%), C_{MM} and C_{CF} increased approximately 5 times and 14 times (71.44%/14.56% and 26.74%/1.96%), respectively.

### 3.2. The Conducted EMI Experiment

The experiment was performed by applying voltage dips directly to the FPGAs V_{DD} pins according to the IEC 61.000-4-29 Normative [7]. Then, we induced voltage dips of 37% to the 3.3V pins feeding the periphery (I/O pads) and 41% to the 1.2V pins feeding the core logic of the FPGA. These voltage dips were injected in the FPGA V_{DD} pins at a frequency range varying from 4 to 14 MHz. Based on these conditions, the resulting V_{DD} fluctuated from ~3.3V to ~2.11V (for the periphery) and from ~1.2 to ~0.75V (for the logic core). For larger voltage dips, the FPGA IC looses configuration and collapses. Fig. 8 displays the injected noise captured with an oscilloscope at the FPGA V_{DD} input pins.

In summary, while C_{CR} was reduced to zero, C_{MM} reduced approximately 7 times (34.18%/4.76%) and C_{CF} was increased approximately 10 times (95.24/9.45%).

![Fig. 8. IEC 61.000-4-29-compliant injected noise captured with oscilloscope at the FPGA V_{DD} input pins.](image)

![Fig. 9. Summary for the IEC 61.000-4-29-based experiment.](image)

### 3.3. Comparing the Approach Effectiveness for Radiated x Conducted EMI

By compiling the measured numbers presented in Sections 3.1 and 3.2, Fig. 10, Table 1 and Fig. 11 summarize the CDC-Modulation Technique effectiveness for improving processor immunity to conducted and radiated EMI.

![Fig. 10. Comparing the CDC-Modulation Technique effectiveness for improving processor immunity to conducted and radiated EMI.](image)

By observing these figures and table, one can conclude the following:

1. When comparing the processor behavior under the conducted versus radiated EMI environments (Fig. 10), the proposed technique yields larger benefits from improving the processor immunity to conducted EMI (84.7% reduction of fault occurrence) than for radiated EMI (39.4%). This reasoning can be explained by the fact that since the CDC-Modulation technique controls the clock signal duty cycle as a reaction to...
power-supply fluctuations, it is mostly expected that when the conducted EMI degrades power-supply integrity, the technique yields the best responses. On the other hand, when radiated EMI affects the processor, the whole circuit gets buried into a “noise wave” that is conducted not only towards the \( V_{DD} \) FPGA pins, but towards all the I/O chip pins (including data and control input paths). This scenario is much more hostile than the former one, where only the FPGA \( V_{DD} \) input pins are mostly degraded.

<table>
<thead>
<tr>
<th>TASK</th>
<th>Multiplier Block Usage Rate</th>
<th>CDC-Modulation Technique Effectiveness (8 of faults occurred during the task execution divided by the overall faults occurred in the system for the CDC-Modulation Version, taking as reference the Original Version)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CF</td>
<td>a few times</td>
<td>Conducted EMI Test: increased approx. 10 times; Radiated EMI Test: increased approx. 14 times</td>
</tr>
<tr>
<td>MM</td>
<td>moderate</td>
<td>Conducted EMI Test: reduced approx. 7 times; Radiated EMI Test: increased approx. 5 times</td>
</tr>
<tr>
<td>CR</td>
<td>intense</td>
<td>Conducted EMI Test: problem eliminated; Radiated EMI Test: reduced approx. 46 times</td>
</tr>
</tbody>
</table>

Table 1. Comparing the CDC-Modulation Technique effectiveness for improving processor immunity to conducted and radiated EMI, displayed as a function of the application tasks.

![Fig. 11. Effectiveness of the CDC-Modulation Technique as a function of the Multiplier Block Usage Rate.](image)

(2) The use of the CDC-Modulation Technique improves processor immunity to conducted and to radiated EMI as well: as more intensive is this usage, the more is the benefit. This situation is illustrated in Table 1 and Fig.11 by the Multiplier Block usage rate: application CR is the one that best benefited from using the proposed technique (during the conducted EMI test, no faults were observed; whereas during the radiated EMI test, the faults occurrence during CR execution with respect to the overall system failures was reduced by a factor of approximately 46 times). Similar reasoning can be applied to MM and CF tasks, where a “moderate” and “a few times” execution rates were applied to the processor Multiplier Block, respectively.

4. CONCLUSIONS

This paper compared the effectiveness of a Clock Duty-Cycle (CDC) Modulation technique to enhance SoC signal integrity with respect to two different disturbance sources: power-supply voltage transients and radiated electromagnetic interference (EMI). The technique is based on a clock stretching logic (CSL) block, which monitors abnormal power grid activity and dynamically (and temporarily) increases CDC of the logic whose power-supply is under disruption.

Practical experiments based on a 32-bit soft-core pipeline processor implemented with the proposed technique and running in a FPGA IC were performed. From these experiments, two main conclusions can be taken:

1. The use of the proposed technique improves SoC immunity to conducted and to radiated EMI as well: as more intensive is this usage during processor run, the more is the benefit.

2. When comparing the processor behavior under the conducted versus radiated EMI environments, the proposed technique yields larger benefits from improving the SoC immunity to conducted EMI (84.7% reduction of fault occurrence) than for radiated EMI (39.4%). This reasoning can be explained by the fact that since the CDC-Modulation technique controls the clock signal duty cycle as a reaction to power-supply fluctuations, it is mostly expected that when the conducted EMI degrades power-supply integrity, the technique yields the best responses. On the other hand, when radiated EMI affects the IC, the whole circuit gets buried into noise that is conducted not only towards the \( V_{DD} \) FPGA pins, but towards all the I/O chip pins (including data and control input paths). This scenario is much more hostile than the former one, where only the FPGA \( V_{DD} \) input pins are mostly degraded.

REFERENCES