Power-Supply Instability Aware Clock Signal Modulation for Digital Integrated Circuits


Abstract - As IC technology scales down, interconnect issues are becoming one of the major concerns of gigahertz System-on-Chip (SoC) design. Voltage distortion (power supply noise) and delay violations (signal and clock skews) dramatically contribute to signal integrity loss. As a consequence, performance degradation, reliability problems and ultimately, functional error occur. In this paper, we propose a new methodology to enhance SoC signal integrity with respect to power/ground voltage transients, without degrading its performance. The underlying principle of the proposed methodology is to dynamically adapt the clock duty-cycle (CDC) according to the signal propagation delay through the logic whose power supply voltage is being disturbed. The methodology is based on a clock stretching logic (CSL) block, which monitors abnormal power grid activity and increases clock duty-cycle accordingly. Moreover, a model to accurately quantify CDC stretching as a function of \( V_{DD}/Gnd \) fluctuations is proposed. Practical experiments based on the implementation of a 32-bit pipeline processor in an FPGA IC were performed and demonstrate the circuit robustness enhancement to power line fluctuations while maintaining at-speed clock rate.

1. INTRODUCTION

Signal integrity is the ability of a signal to generate correct responses in a circuit. It generally includes all effects that cause a circuit malfunction due to the distortion of the signal waveform [1]. According to this definition, a signal with good integrity presents: (i) voltage values at required levels and (ii) level transitions at required times. For instance, an input signal to a flip-flop with good signal integrity arrives early enough to guarantee the setup and hold times and it does not have spikes that may cause undesired logic transitions.

Various signal integrity problems have been studied for high-speed gigahertz nanometer System-on-Chip (SoC). The most important ones are: (a) crosstalk (signal distortion due to cross coupling effects between signals) [2,3]; (b) overshoot/undershoot (momentarily signal rising/decreasing above/below the power supply voltage (\( V_{DD} \)) and ground (\( V_{SS} \)) lines) [4,5]; (c) reflection (echoing back a portion of a signal, at high-frequency circuits, where interconnections behave as transmission lines); (d) electromagnetic interference – EMI (resulting from antenna properties) [6,7,24]; (e) power-supply noise [8,9]; and (f) signal skew (delay in arrival time to different receivers) [10-12].

In this work, we are concerned with the power supply disturbances, regardless of their origin, and their impact on digital circuit performance. Both \( V_{DD} \) depletion and ground elevation cause propagation delay through signal path increase. It is assumed that well-known techniques [13,14] are used to limit the impact of power supply disturbances on clock generation and distribution performance. In this scenario, if a signal propagation delay is large enough, it will induce a de-synchronization effect due to the increased difference between the critical path propagation delay and the clock distribution network delay. Hence, e.g., 10% power supply voltage fluctuations may translate in more than 10% timing inaccuracy, causing a functional error [12]. Moreover, noise margins are reduced in the presence of power-supply voltage transients. This problem gets worse with technology scaling down. Interestingly, research results on delay fault detection and diagnosis can be reused to enhance delay fault tolerance (and thus signal integrity) to power supply voltage transients [15].

Many design and fabrication solutions have been proposed to enhance signal integrity in the presence of power grid activity. However, none of them guarantees perfect solution for the de-synchronization effect described above. In addition to the uncertainties that result from using these solutions, their use often requires the knowledge of the instantaneous maximum power supply current, \( I_{DD}(t) \), for delay analysis (as opposed to power dissipation that relates to average current). The estimation of this parameter for complex designs is frequently a burden task, since it is strongly dependent on input-pattern sequence, even if the output is not switching. Some of the proposed solutions include: 3-D layout modeling and parasitic extraction [16]; accurate RLC simulation of on-chip power grid [10] using decoupling
capacitors [8,17] to improve resistive voltage drop (IR-drop) [10,18]; insertion of buffers on the grid [16]; and shielding wires (e.g., grounding every other line) [19]. Buffer insertion and transistor resizing methods have also been proposed [20,21] to achieve better power-delay and area-delay trade-offs. Additionally, self-test methodologies and on-chip probes to monitor intra-packaging EM-emission activities [22] have been developed to test signal integrity in high-speed SoC. Finally, other techniques have been discussed in the literature [24]. For example, the reduction of the maximum distance between supply pins and the circuit supply connections [23]. This can be achieved, for instance, by implementing finger-shaped power distribution networks to feed $V_{DD}$ and ground signals throughout the internal blocks of the IC.

Undesired voltage transients in power/ground interconnects may be constrained, but not eliminated completely. In order to guarantee correct timing performance in their presence, the ultimate solution is to reduce the clock signal frequency. For some applications, such performance loss cannot be tolerated. Hence, for a significant set of applications, a new solution must be searched for, which is not based on the clock frequency reduction. The underlying principle of the proposed methodology is to dynamically adapt the clock duty-cycle (CDC) according to the signal propagation delay through the logic whose power supply voltage is being disturbed. The functionality to implement the underlying principle is as follows: (1) power supply voltage monitoring and (2) when voltage variation exceeds a user's defined threshold, CDC modulation. Hence, the correspondent architecture contains a clock stretching logic (CSL) block, to monitor power grid activity ($V_{DD}$ undershoots and/or ground overshoots) and to enhance the clock duty-cycle provided by the phase-locked loop (PLL) block to the controlled logic when required.

Therefore, the main advantage of the proposed methodology is to render the circuit more robust to power line fluctuations by maintaining at-speed clock rate. As such fluctuations are often due to circuit operation, they tend to cause local disturbances in the power grid. Hence, it is a waste to reduce the clock frequency in the overall system. The proposed methodology locally adapts the CDC without loosing circuit performance.

### 2. CLOCK DUTY CYCLE MODULATION

As referred, lowering the power supply voltage, $V_{DD}$, enhances the propagation delay of signal paths. Hence, if the observation pace is kept invariant (at-speed circuit operation), lowering $V_{DD}$ while maintaining nominal clock period, $t_{CL}$, reduces circuit noise and time margins, which will, ultimately, induce system functional errors. The time margin is characterized by the time slack, $t_{spy}$. In this work, the time slack is defined as the time interval difference between the clock period and the time interval associated with the time response of the critical path in the slowest combinational module between registers.

Let us also consider another phenomenon, the ground bounce, also known as simultaneous switching noise. This phenomenon occurs when internal nodes of a logic device change state. When this happens, the charge remaining in the internal nodes ($C_i$) is drained through the ground grid. The currents associated with this charge removal are added to the switching currents flowing from $V_{DD}$ to the ground interconnects due to the simultaneous switching of the N- and P-networks. Thus, the resulting total current flowing through the ground grid induces a local voltage variation, namely, the ground bounce, $V_{GB}$. Worst-case conditions exist when a large number of nodes simultaneously switch. In this case, the resulting switching currents from each node capacitance are added together. The total current flowing through the ground lead reduces noise margins and increases the probability of system malfunction.

For the sake of simplicity, we normalize the size of the disturbance on $V_{DD}$/Gnd interconnects voltage using a gamma parameter:

$$\gamma(vdd) = \frac{\Delta V_{DD}}{V_{DD\text{nom}}} \quad \text{or} \quad \gamma(gnd) = \frac{\Delta V_{GND}}{V_{GND\text{nom}}}$$

where: $\Delta V_{DD}$ is the difference between the nominal $V_{DD}$ ($V_{DD\text{nom}}$) and the depleted $V_{GP}$, and $\Delta V_{GND} = \Delta V_{SS}$ is the difference between the elevated ground and $V_{SS} = 0$ Volt.

### 3. PROPOSED METHODOLOGY

The proposed methodology is based on the following assumptions:

- a) CDC is generally set at 50% to minimize the jitter effect and uncertainties associated with parameters spread due to process variations; and to allow a weighted-time distribution for circuits designed with both rise- and fall-edge triggered flip-flops.
- b) The maximum value to which CDC can be stretched is significantly lower than 100% (otherwise, the combinational logic part collapses). In practice, the maximum allowed value is 80%.
- c) CDC may be temporarily modified for some functional parts of a SoC, but maintained unchanged for the other parts. This does not result in circuit functional error if the overall clock rate is kept unchanged and all the combinational parts of the circuit keep working synchronously.

Consider a synchronous IP core, with different modules, each fed by a subsection of the power grid infrastructure (Fig. 1). If circuit operation induces $V_{DD}$ variations in module $i$, its timing performance is distorted, typically delayed. In order to allow the combinational blocks to finish their job, an additional time has to be given to the signals switching in critical paths. Hence, the underlying idea is to dynamically delay their capture, by the critical memory cells, in the presence of $V_{DD}$ variation. Therefore, for a limited subset of the module’s registers ($m < k$), a CDC modulation block must be added to accommodate such delay.

In a synchronous circuit, CDC is generally set at 50% to minimize jitter and process variations, and to allow a weighted-time distribution for circuits designed with both rise- and fall-edge triggered flip-flops (FF). In order to prevent logic errors, we assume that CDC may be stretched up to 80%.

We refer as CDCM (or CDC Modulation) module the one that implements this added functionality. Locally, the CDCM module monitors $V_{DD}$ variations and triggers CDC variations accordingly. For each IP module, static timing analysis is used to identify the critical paths,
allowing us to determine how many CDC modulators should be inserted (and where). Here, we illustrate the methodology using one power grid partition, one functional module and one CDCM system.

As shown in Fig. 2, the proposed CDCM architecture is based on a clock stretching logic (CSL) block, which monitors power grid activity and enhances the clock signal (CLK) delivered by the phase-locked loop (PLL) block to the controlled logic accordingly. In this architecture, the CDCM module performs disturbance monitoring and CDC stretching using a simple circuit and introducing a limited clock delay, τ₁, (referred to as the intrinsic CDCM delay). The modulated clock signal adds a minimum stretch at nominal V_DD (CDC slightly greater than 50%). When V_DD decreases, the CSL block stretches CDC according to V_DD reduction. In this case, the time slack is increased by the amount τ₂, i.e., τ = τ₁ + τ₂. When the V_DD voltage transient fades away, the CSL block starts gradually reestablishing the original clock duty-cycle (50%) to the controlled logic (Critical Memory Cells).

Several architectures for the CSL block can be implemented. One possible implementation in static CMOS technology is shown in Fig. 3. The CSL block modulate CDC by delaying one of the switching transitions (in this case, the High-to-Low transition). The M1-M2 inverter implements the CDC modulator core. Its pull-up PMOS transistor (M2) has a slow driving capability, due to M3. The result is a modulated clock signal, with identical clock period, but with enhanced CDC in the presence of a reduction of V_DD. The output signal is buffered to restore the fast switching capability. For circuits with both rising and falling-edge trigger clocks, two types of CSL circuits must be implemented.

In Fig. 4, simulation results (AMS 350 nm CMOS technology) show the CSL block capability to stretch CDC proportionally to V_DD depletion, from nominal V_DD (3.3 Volt) down to V_DD = 1.0 Volt. Note that the stretched CDC is always larger than 50% and lower than 100%. When V_DD is depleted to the lowest possible value (1.1V) CDC reaches 79%. Below 1.1 V, the correct functionality collapses.

### 3.1. CDC Modulation Model

A model to accurately quantify CDC stretching as a function of V_DD/V_SS fluctuations has been developed. The amount of CDC variation, required to tolerate a given V_DD variation, depends on the designer’s defined time slack value, t_PM. Typically, it may correspond, for nominal values of the circuit parameters, to 8-10% of T_PM, the time period required by the longest critical path to propagate the switching values. When the power supply range, (V_DD - V_SS) decreases, it erodes t_PM. One part of the speed degradation may be “absorbed” by the reduction in t_PM, without causing a functional error; however, if this occurs, there is no guarantee of correct functionality. Therefore, in our approach, CDC variation, required to tolerate V_DD variation, must preserve the nominal t_PM value. If t_CLK is the clock signal period, then

\[ t_{CLK} = T_{pd} + t_{PM} \]  

(2)  

In the absence of CDC modulation, CDC=50% and thus

\[ CDC = T_{in} / t_{CLK} = 50\% \]  

(3)  

where T_{in} is the time interval in which the clock signal assumes the ‘1’ logic value. When a Δ V_DD occurs, a new value of CDC, referred as CDC', must be applied. In the worst-case situation (for which nominal t_PM is kept), the clock duty cycle...
must stretch by the same amount of time required for signal propagation through the logic path. Hence,

\[
CDC' = \left( T_{\text{on}} + T_{\text{pd}} \Delta T_{\text{pd}} \right) / t_{\text{CLK}}
\]  

and

\[
\Delta CDC (V_{DD}) = CDC' - CDC = \left[ T_{\text{pd}} / t_{\text{CLK}} \right] \Delta T_{\text{pd}} (V_{DD})
\]

As a consequence, CDC maximum variation follows \( T_{\text{pd}} (V_{DD}) \) variation, for which the authors have previously developed a simple analytical model [12,15]. The typical architecture of the CSL block, depicted in Fig. 4, allows deriving such variation.

4. EXPERIMENTAL RESULTS

Practical experiments were performed on a 32-bit microprocessor that was mapped into an FPGA IC. Aiming at demonstrating the proposed approach effectiveness, these experiments are described hereafter.

We selected the PLASMA soft-core microprocessor which was retrieved from the Internet public domain “Opencores” [26]. This is a 32-bit three-stage pipeline processor described in VHDL and mapped into a test board [25] previously designed and implemented by the authors. Fig. 5 depicts the PLASMA general architecture and its VHDL basic blocks. This processor was downloaded into the test board shown in Fig. 6. This is a six-layer board designed and fabricated in partial compliance with the standard IEC 62.132 for radiated and conducted electromagnetic (EM) immunity measurements.

![Fig. 5. PLASMA processor: (a) general architecture, and (b) VHDL basic blocks used to describe the processor.](image)

Among the facilities available in this board, there is a temperature sensor that allows us to perform a burn-in test in conjunction with IEC test sessions [25]. Additionally, the 2 FPGAs, 4 SRAMs, 2 Flashes and the 8051 microcontroller have separated power-supply bus. This infrastructure allows us to perform individual RF-conducted noise injection into any of these ICs, or any combination of them. To do so, a second board (not shown in Fig. 7) containing special connectors for RF-conducted noise injection is attached to the periphery pins of the board shown in Fig. 7b.

Two versions of this processor were implemented and prototyped in one of the FPGAs of Fig. 6a. The first version (namely, “Original”) had the CDC fixed to 50% during the whole experiment. The second version (“CDC-Modulation”) had the CDC controlling the Multiplier Block modulated during the test session. To do so, we modified the VHDL code describing the PLASMA by adding an external pin to the processor so that we were able to control the CDC addressing the Multiplier Block. The remaining blocks of the processor had the CDC fixed to 50%. The CDC was modified in such a way that when the modulation was activated, the rising edge of the clock signal was delayed. The Original and the CDC-

\[ ^{2} \text{IEC 62.132, IEC 61.004-17 and IEC 61.004-29.} \]
Modulation processor versions were prototyped into separate FPGAs on the “test side” of the board (Fig. 6a), so that the same tasks and input vectors were simultaneously applied to both processors running in parallel during the experiment. Note that:

1) We selected the Multiplier Block to have the CDC controlled because this block was the only one in the PLASMA description (Fig. 6c) that had explicit clock signal declaration in the VHDL code. For the PLASMA remaining blocks, the clock signal was declared as asynchronous actions triggered after the instruction decoding from the Control Block. So, if other processor blocks had to be controlled, we would have to carry out complex changes in the VHDL code.

2) All the D flip-flops (D-FFs) in the Original VHDL code of the Multiplier Block were declared as the type “rising-edge D-FFs”. So, when the CSL block modulated the clock signal in the CDC-Modulation VHDL version, it actually reduced the CDC from 50% to 25%. This action was carried out by delaying the rising-edge of the clock signal. Thus, it delayed the D-FFs triggering instant. Fig. 7 depicts this situation.

The experiment was performed by applying voltage dips to the FPGAs VDD pins according to the IEC 61.000-4-29 International Std. Normative [25]. Then, we induced voltage dips of 37% to the 3.3V pins feeding the periphery (I/O pads) and 41% to the 1.2V pins feeding the core logic of the FPGA. These voltage dips were injected in the FPGA pins at a frequency range varying from 4 to 14 MHz. Based on this condition, the resulting VDD fluctuated from ~3.3V to ~2.11V (for the periphery) and from ~1.2 to ~0.75V (for the logic core). We tried also to apply deeper voltage dips, but the FPGA IC lost configuration and collapsed. Fig. 8 displays the injected noise captured with the oscilloscope at the FPGA VDD input pins.

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Fig. 9 summarizes the measured output values for the processor. For this experiment, the processor executed (in a time-shared basis) three application tasks under the control of its native operating system: Multiplication Matrix (MM), Curve Fitting (CF) and Cryptography (CR). The experiment was arranged in such a way that the PLASMA executed the three tasks with the same priority. This condition allocated 33% of the CPU time to run each of the tasks. A shown in Fig. 9a, the use of the CDC-Modulation technique hardened the processor by an average factor of 84.73% ([275-42]/275.100%).

Additionally, the usage of the Multiplier Block by the tasks was intentionally made not equal: task CR was the one that used intensively this hardware resource. Next, the MM task was implemented in such a way to use it moderately. Finally, the CF was the application task that least used the Multiplier Block. As shown in Fig. 9b, this Multiplier Block usage condition was reflected in terms of CDC-Modulation effectiveness: the fault occurrence relative contribution of the CR task with respect to the overall faults that occurred in the system was reduced from 56.36% ([155/275].100%) in the Original Plasma version to zero in the CDC-Modulation version. For the MM task, its fault occurrence relative contribution with respect to the overall faults that occurred in the system was reduced from 34.18% ([94/275].100%) in the Original Plasma version to 4.76% ([40/42].100%) in the CDC-Modulation version. Finally for the CF task, its fault occurrence relative contribution with respect to the overall faults that occurred in the system was increase from 9.45% ([26/275].100%) in the Original Plasma version to 95.24% ([40/42].100%) in the CDC-Modulation version.

In other words, while the CR task had its contribution in the system failure reduced to zero, the MM task had its participation in the system disruption reduced by ~7X (34.18%/4.76%) and the CF application increased its participation by ~10X (95.24/9.45%).
5. CONCLUSIONS

It was presented a new methodology aiming at enhancing SoC signal integrity to power-supply fluctuations. The goal is to keep circuit synchronism and nominal performance even in the presence of \( V_{DD}/V_{GND} \) disturbances that, due to increased signal path delays, may cause IC de-synchronization. Typical solutions define, during design phase, conservative (reduced) IC clock rates to ensure synchronization between signal propagation through logic with clock control under power-supply grid disturbance.

The methodology is based on a clock duty cycle modulation (CDCM) concept, which is built-up around a clock stretching logic (CSL) block. The CSL is used to monitor abnormal power interconnect activities (\( V_{DD} \) undershoots or ground overshoots) and to enhance CDC proportionally to supply voltage variation. This solution is implemented by delaying the rising (or falling) edge of the clock signal, depending on which kind of D-FF is used in the controlled logic. A typical implementation of the CSL block was proposed. The range of the CDC variation to tolerate \( V_{DD} \) disturbance has also been identified and discussed.

Experimental results based on the implementation of a 32-bit pipeline microprocessor into a FPGA demonstrate the effectiveness of the proposed methodology to react to power-supply fluctuations by stretching the clock signal fed to the controlled logic. It is a primary condition that the CSL block must be, by design, more robust to power supply voltage transients than the logic to be controlled. As shown in Section 3, Fig. 4, by carefully adjusting internal CSL block parameters it is possible to reach self-tolerance to power-supply oscillation up to 50% (\( \gamma(V_{DD}) = 67\% \)). It is worth noting that, as expected for any logic, this tolerance is operating frequency-dependent: as higher as operating clock rates are, less tolerant is the CSL block to \( V_{DD} \) oscillations.

REFERENCES


