Measuring Clock-Signal Modulation Efficiency for Systems-on-Chip in Electromagnetic Interference Environment


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Abstract

As IC technology scales down, signal integrity issues such as power supply noise and clock skews are becoming one of the major concerns of gigahertz System-on-Chip (SoC) design. Considering that one of the most important mechanisms to degrade signal integrity is electromagnetic interference (EMI), this paper2 analyzes the effectiveness of a Clock Duty-Cycle (CDC) Modulation technique to enhance SoC signal integrity with respect to power/ground voltage transients induced by EMI. The technique is based on a clock stretching logic (CSL) block, which monitors abnormal power grid activity and increases CDC accordingly. Practical experiments based on the implementation of a 32-bit soft-core pipeline processor in an FPGA IC were performed and illustrate the circuit robustness enhancement to power line fluctuations while maintaining at-speed clock rate. These experiments were conducted according to the IEC 62.132-2 Normative for measurement of radiated electromagnetic immunity (TEM-cell method).

1. INTRODUCTION

Signal integrity is the ability of a signal to generate correct responses in a circuit. It generally includes all effects that cause a circuit malfunction due to the distortion of the signal waveform [1]. According to this definition, a signal with good integrity presents: (i) voltage values at required levels and (ii) level transitions at required times. For instance, an input signal to a flip-flop with good signal integrity arrives early enough to guarantee the setup and hold times and it does not have spikes that may cause undesired logic transitions.

Various signal integrity problems have been studied for high-speed gigahertz nanometer System-on-Chip (SoC). The most important ones are: (a) crosstalk (signal distortion due to cross coupling effects between signals) [2,3]; (b) overshoot/undershoot (momentarily signal rising/decreasing above/below the power supply voltage (VDD) and ground (VSS) lines) [4,5]; (c) reflection (echoing back a portion of a signal, at high-frequency circuits, where interconnections behave as transmission lines); (d) power-supply noise [8,9]; and (e) signal skew (delay in arrival time at different receivers) [10-12].

With no exception, any of these signal integrity problems can be caused by electromagnetic interference (EMI). The mechanism by which EMI affects electronics can be explained by the fact that high-frequency IC internal tracks and devices, board-level tracks, pins, connectors and cables can behave according to antenna properties, so thus to emit or capture radio-frequency (RF) energy [6,7,24]. Power-supply grid and clock-signal network are one of the best examples of structures behaving like antennas at the IC level (for signals in the order of 10 GHz) and also at the board level (for signals at 100 MHz). As consequence, the electromagnetic (EM) environment in which SoCs have to operate is becoming increasingly hostile while our dependence on electronics is widespread and increasing. The need for insuring that application upsets due to the EM environment will not occur is fundamental to acceptance of systems as fit for purpose. Thus, it is important to understand how future technologies impact on next-generation complex systems-on-chips (SoCs). Note that although the reduction of supply voltages (at least for the core part) rises the hope for less EM emission (conducted and radiated), this benefit is immediately compensated by a:

(a) drastically increased number of simultaneously switching transistors per die, combined with faster switching edges due to increasing clock rates. Thus, increasing the total RF noise that can affect embedded functional blocks inside the die itself, as well as affecting other dies or ICs placed nearby it;

(b) reduction of the noise margins in which the IC was designed to operate. Thus, rendering the IC critical embedded functional blocks more sensitive to EMI.

In this work, we are concerned with power supply disturbances induced by radiated EMI and its impact on the digital circuit performance. More precisely, we are focused on analyzing the effectiveness of the Clock Duty-Cycle (CDC) Modulation technique [7] to enhance signal integrity with respect to power/ground voltage transients when SoCs are exposed to EM environments.

Many design and fabrication solutions have been proposed to enhance signal integrity in the presence of power grid activity. Some of the proposed solutions include: 3-D layout modeling and parasitic extraction [16]; accurate RLC simulation of on-chip power grid [10] using decoupling capacitors [8,17] to improve resistive voltage drop (IR-drop)
[10,18]; insertion of buffers on the grid [16]; and shielding wires (e.g., grounding every other line) [19]. Buffer insertion and transistor resizing methods have also been proposed [20,21] to achieve better power-delay and area-delay trade-offs. Additionally, self-test methodologies and on-chip probes to monitor intra-packaging EM-emission activities [22] have been developed to test signal integrity in high-speed SoC. Finally, other techniques have been discussed in the literature [24]. For example, the reduction of the maximum distance between supply pins and the circuit supply connections [23]. This can be achieved, for instance, by implementing finger-shaped power distribution networks to feed $V_{DD}$ and ground signals throughout the internal blocks of the IC.

All the above mentioned approaches to improve SoC signal integrity can be applied with different degrees of success; however, none of them guarantees perfect solution. In addition to the uncertainties that result from using these approaches, their use often requires the knowledge of the instantaneous maximum power supply current, $I_{DD}(t)$, for delay analysis (as opposed to power dissipation that relates to average current). The estimation of this parameter for complex designs is frequently a burden task, since it is strongly dependent on input-pattern sequence, even if the output is not switching.

In this scenario, the underlying principle of the proposed methodology is to dynamically adapt the CDC according to the signal propagation delay through the logic whose power supply voltage is being disturbed. The functionality to implement this principle is as follows: (1) power supply voltage monitoring and (2) when voltage variation exceeds a user’s defined threshold, CDC modulation. Hence, the correspondent architecture contains a clock stretching logic (CSL) block, to monitor power grid activity ($V_{DD}$ undershoots and/or ground overshoots) and to enhance the clock duty-cycle provided by the phase-locked loop (PLL) block to the controlled logic when required.

The main advantage of the proposed methodology is to render the circuit more robust to power line fluctuations by maintaining at-speed clock rate. As such fluctuations are often due to circuit operation, they tend to cause local disturbances in the power grid. Hence, it is a waste to reduce the clock frequency in the overall system. The proposed methodology locally adapts the CDC without losing circuit performance.

2. CLOCK DUTY CYCLE MODULATION

As referred, lowering the power supply voltage, $V_{DD}$, enhances the propagation delay of signal paths. Hence, if the observation pace is kept invariant (at-speed circuit operation), lowering $V_{DD}$ while maintaining nominal clock period, $t_{CLK}$, reduces circuit noise and time margins, which will, ultimately, induce system functional errors. The time margin is characterized by the time slack, $t_{PM}$. In this work, the time slack is defined as the time interval difference between the clock period and the time interval associated with the time response of the critical path in the slowest combinational module between registers.

Let us also consider another phenomenon, the ground bounce, also known as simultaneous switching noise. This phenomenon occurs when internal nodes of a logic device change state. When this happens, the charge remaining in the internal nodes ($C_L$) is drained through the ground grid. The currents associated with this charge removal are added to the switching currents flowing from $V_{DD}$ to the ground interconnects due to the simultaneous switching of the N- and P-networks. Thus, the resulting total current flowing through the ground grid induces a local voltage variation, namely, the ground bounce, $V_{GB}$. Worst-case conditions exist when a large number of nodes simultaneously switch. In this case, the resulting switching currents from each node capacitance are added together. The total current flowing through the ground lead reduces noise margins and increases the probability of system malfunction.

3. PROPOSED METHODOLOGY

The proposed methodology is based on the following assumptions:

a) CDC is generally set at 50% to minimize the jitter effect and uncertainties associated with parameters spread due to process variations; and to allow a weighted-time distribution for circuits designed with both rise- and fall-edge triggered flip-flops;

b) The maximum value to which CDC can be stretched is significantly lower than 100% (otherwise, the combinational logic part collapses). In practice, the maximum allowed value is 80%.

c) CDC may be temporarily modified for some functional parts of a SoC, but maintained unchanged for the other parts. This does not result in circuit functional error if the overall clock rate is kept unchanged and all the combinational parts of the circuit keep working synchronously.

Consider a synchronous IP core, with different modules, each fed by a subsection of the power grid infrastructure (Fig. 1). If circuit operation induces $V_{DD}$ variations in module $i$, its timing performance is distorted, typically delayed. In order to allow the combinational blocks to finish their job, an additional time has to be given to the signals switching in critical paths. Hence, the underlying idea is to dynamically delay their capture, by the critical memory cells, in the presence of $V_{DD}$ variation. Therefore, for a limited subset of the module’s registers ($m < k$), a CDC modulation block must be added to accommodate such delay.

In a synchronous circuit, CDC is generally set at 50% to minimize jitter and process variations, and to allow a weighted-time distribution for circuits designed with both rise- and fall-edge triggered flip-flops (FF). In order to prevent logic errors, we assume that CDC may be stretched up to 80%.

We refer to as CDCM (or CDC Modulation) module the one that implements this added functionality. Locally, the CDCM module monitors $V_{DD}$ variations and triggers CDC variations accordingly. For each IP module, static timing analysis is used to identify the critical paths, allowing us to determine how many CDC modulators should be inserted (and where). Here, we illustrate the methodology using one power grid partition, one functional module and one CDCM system.
As shown in Fig. 2a, the proposed CDCM architecture is based on a clock stretching logic (CSL) block, which monitors power grid activity and enhances the clock signal (CLK) delivered by the phase-locked loop (PLL) block to the controlled logic accordingly. In this architecture, the CDCM module performs disturbance monitoring and CDC stretching using a simple circuit and introducing a limited clock delay, $\tau_m$, (referred to as the intrinsic CDCM delay). During normal operation (nominal $V_{DD}$), the CSL delivers a modulated clock signal ($CLK_{CDCM}$) with a CDC around 50%. When $V_{DD}$ decreases, the CSL block stretches CDC according to $V_{DD}$ reduction. In this case, the time slack ($\tau_{m}$) is increased by an amount $\tau'_m$, i.e., $\tau_{m}' = \tau_{m} + \tau(V_{DD})$. When the $V_{DD}$ voltage transient fades away, the CSL block starts gradually reestablishing the original clock duty-cycle (50%) to the controlled logic (in Critical Memory Cells). Fig. 2b illustrates the two possible ways of stretching the CDC (delaying the rising edge or delaying the falling edge) depending on the type of the critical memory cells used.

Several architectures for the CSL block can be implemented. One possible implementation in static CMOS technology is shown in Fig. 3. The CSL block modulates CDC by delaying one of the switching transitions (in this case, the High-to-Low transition). The M1-M2 inverter implements the CDC modulator core. Its pull-up PMOS transistor (M2) has a slow driving capability, due to M3. The result is a modulated clock signal, with identical clock period, but with enhanced CDC in the presence of a reduction of $V_{DD}$. The output signal is buffered to restore the fast switching capability. For circuits with both rising and falling-edge trigger clocks, two types of CSL circuits must be implemented.

In Fig. 4, simulation results (AMS 350 nm CMOS technology) show the CSL block capability to stretch CDC proportionally to $V_{DD}$ down to $V_{DD} = 1.0$ Volt. Note that the stretched CDC is always larger than 50% and lower than 100%. When $V_{DD}$ is depleted to the lowest possible value (1.1V) CDC reaches 79%. Below 1.1 V, the correct functionality collapses.

**3.1. CDC Modulation Model**

A model to accurately quantify CDC stretching as a function of $V_{DD}/V_{SS}$ fluctuations has been developed. The amount of CDC variation, required to tolerate a given $V_{DD}$ variation, depends on the designer’s defined time slack value, $\tau_{PM}$. Typically, it may correspond, for nominal values of the circuit parameters, to 8-10% of $T_{pd}$, the time period required by the longest critical path to propagate the switching values. When the power supply range, $(V_{DD} - V_{SS})$ decreases, it erodes $\tau_{PM}$. One part of the speed degradation may be “absorbed” by the reduction in $\tau_{PM}$, without causing a functional error; however, if this occurs, there is no guarantee of correct functionality. Therefore, in our approach, CDC variation, required to tolerate $V_{DD}$ variation, must preserve the nominal $\tau_{PM}$ value. If $t_{CLK}$ is the clock signal period, then

$$t_{CLK} = T_{pd} + \tau_{PM}$$  \hspace{1cm} (1)
In the absence of CDC modulation, CDC=50% and thus
\[ \text{CDC} = \frac{T_{on}}{t_{CLK}} = 50\% \]  
where \( T_{on} \) is the time interval in which the clock signal assumes the ‘1’ logic value. When a \( \Delta V_{DD} \) occurs, a new value of CDC, referred as CDC, must be applied. In the worst-case situation (for which nominal \( t_{pd} \) is kept), the clock duty cycle must stretch by the same amount of time required for signal propagation through the logic path. Hence,
\[ \text{CDC}' = \left( T_{on} + t_{pd} \Delta T_{pd} \right) / t_{CLK} \]  
and
\[ \Delta \text{CDC} (V_{DD}) = \text{CDC}' - \text{CDC} = \frac{t_{pd}}{t_{CLK}} \Delta T_{pd} (V_{DD}) \]  
As a consequence, CDC maximum variation follows \( T_{pd}(V_{DD}) \) variation, for which the authors have previously developed a simple analytical model [12,15]. The typical architecture of the CSL block, depicted in Fig. 4, allows deriving such variation.

4. EXPERIMENTAL RESULTS

Practical experiments were performed on a 32-bit microprocessor that was mapped into a FPGA IC. Aiming at demonstrating the proposed approach effectiveness, these experiments are described hereafter.

We selected the Plasma soft-core microprocessor which was retrieved from the Internet public domain “Opencores” [14]. This is a 32-bit three-stage pipeline processor described in VHDL and mapped into a test board previously designed and implemented by the authors. Fig. 5 depicts the Plasma general architecture and its VHDL basic blocks. This processor was downloaded into the test board shown in Fig. 6. This is a six-layer board designed and fabricated in partial compliance with the standard IEC 62.132 for radiated and conducted electromagnetic (EM) immunity measurements [13].

![Fig. 5. General architecture of the soft-core Plasma processor [14].](image)

The devices under test: 2 FPGAs (Xilinx Spartan 500E), 4 SRAMs, 2 Flashes and the 8051 microcontroller (including the Plasma processor mapped into these FPGAs) are placed on the so called “test side” of the board (Fig. 6a). This side contains also the ground layer of the board. The remaining control logic (a third FPGA, a second 8051 microcontroller, clock signal generators, reset-push bottoms, serial-communication connectors, and dedicated I/O pins for data monitoring and power-supply injection) are mounted on the “other side” of the board (Fig. 6b). This board side also lays down the \( V_{DD} \) distribution network for the system. The four board inner layers are used for signal routing.

![Fig. 6. General view of the IEC-compliant test board used to prototype the Plasma processor: (a) test side, (b) the remaining glue logic, (c) block diagram.](image)

Among the facilities available in this board, there is a temperature sensor that allows us to perform a burn-in test in conjunction with IEC test sessions [13]. Additionally, the devices on the “test side” have separated power-supply bus. This infra-structure allows us to individually control the voltage level provided to the \( V_{DD} \) (resp. Gnd) bus of each of these ICs. Similarly, we can also perform individual RF-conducted noise injection into any of these ICs or combination of them through these dedicated power busses on the “test side”. To do so, a dedicated board (not shown in Fig. 6) containing special connectors for RF-conducted noise injection is attached on the periphery pins of the board shown in Fig. 6b.

Two versions of the Plasma processor were implemented and mapped into the FPGAs of the “test side”. The first version (namely, “Original”) had the CDC fixed to 50% during the whole experiment. The second version (“CDC-Modulation”)

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1 IEC 62.132, IEC 61.004-17 and IEC 61.004-29.
had the CDC controlling the Multiplier Block of the Plasma processor modulated during the test session. To do so, we modified the VHDL code describing the Plasma processor by adding an external pin to the processor so that we could control the CDC addressing the Multiplier Block. The remaining blocks of the processor had the CDC fixed to 50%. The CDC was modified in such a way that when the modulation was activated, the rising edge of the clock signal was delayed. The *Original* and the *CDC-Modulation* processor versions were prototyped into separate FPGAs on the “test side” of the board (Fig. 6a), so that the same tasks and input vectors were simultaneously applied to both processors running in parallel during the experiment. Note that:

1. We selected the Multiplier Block to have the CDC controlled because this block was the only one in the Plasma description (Fig. 5) that had explicit clock signal declaration in the VHDL code. For the Plasma remaining blocks, the clock signal was declared as asynchronous actions triggered after instruction decoding from the Control Part. So, if other processor blocks had to be controlled, we would have to carry out complex changes in the VHDL code.

2. All the D flip-flops (D-FFs) in the *Original* VHDL code of the Multiplier Block were declared as the type “rising-edge D-FFs”. So, when the CSL block modulated the clock signal in the CDC-Modulation VHDL version, it actually reduced the CDC from 50% to 25%. This action was carried out by delaying the rising-edge of the clock signal. Thus, it delayed the D-FFs triggering instant. Fig. 7 depicts this situation.

![Fig. 7. Summary of the original and the stretched clock waveforms: Original clock (clk_50%); Stretched clock activating rising-edge FFs (clk_25%).](image)

Next, the whole set (test board and shielding box) was placed inside the GTEM cell, where the experiment was performed (Figs. 8b and 8c).

The experiment is the result of a total time of system exposition to irradiated EMI of approximated 40 hours. Test conditions were ruled by (but not limited to) the IEC 62.132-2 standard as follows:

- **a)** EM field range: from 10 to 220V/m;
- **b)** Measured frequency range: from 150KHz to 3GHz (extended IEC 62.132-2);
- **c)** Signal Modulation Format: 80%.

Additionally, the two FPGAs containing the *Original* Plasma version and the *CDC-Modulation* version had the power supply pins individually controlled in such a way to render the devices more sensitive to the irradiated EMI. This was obtained by reducing 33% the voltage level feeding the FPGAs’ V_{DD} pins as follows:

- Core: from 1.2V (nominal) to 0.80V.
- Periphery 1: from 2.5V (nominal) to 1.67V.
- Periphery 2: from 3.3V (nominal) to 2.21V.

![Fig. 8. Test environment showing GTEM Cell and test vehicle. (a) General view; (b) and (c) Closer views detailing the test board connected to the shielding box (with the “test side” turned out) into the chamber.](image)

Fig. 8a depicts the test environment used to perform the experiment. The measurements were carried out on a Gigahertz Transverse Electromagnetic (GTEM) Cell, which was used to radiate EMI on the test board. With this goal, the board was placed into a shielding box to prevent the glue logic on the “other side” of the board from being affected by the radiated EMI. Note that the “test side” of the board is placed outwardly the shielding box, so that the devices under test are exposed to the radiation. Then, the whole set (test board and shielding box) was placed inside the GTEM cell, where the experiment was performed (Figs. 8b and 8c).

![Fig. 9. Summary for the IEC 62.132-2-based experiment.](image)

Fig. 9 summarizes the measured output values for the processor. For this experiment, the processor executed (in a time-shared basis) three application tasks under the control of its native operating system: Multiplication Matrix (MM), Curve Fitting (CF) and Cryptography (CR). The experiment was arranged in such a way that the processor executed the three tasks with the same priority. This condition allocated 33% of the CPU time to run each of the tasks. A shown in Fig. 9a, the use of the *CDC-Modulation* technique hardened the processor by an average factor of 39.36% ([1992-1208]/1992].100%).

Additionally, the usage of the Multiplier Block by the tasks was intentionally made not equal: task CR was the one that used intensively this hardware resource. Next, the MM task was implemented in such a way to use it moderately. Finally, the CF
was the application task that least used the Multiplier Block. As shown in Fig. 9b, the Multiplier Block usage condition was reflected in terms of CDC-Modulation effectiveness: the fault occurrence relative contribution of the CR task with respect to the overall faults that occurred in the system was reduced from 83.48% ([1663/1992], 100%) in the Original Plasma version to only 1.82% ([22/1208], 100%) in the CDC-Modulation version. On the opposed direction, the relative contribution of the MM and CF tasks with respect to the overall faults that occurred in the system increased from 14.56% ([290/1992], 100%) and 1.96% ([39/1992], 100%) in the Original Plasma version to 71.44% ([863/1208], 100%) and 26.74% ([323/1208], 100%) in the CDC-Modulation version, respectively.

In other words, while the contribution of the CR task to system failure was reduced ~46X (83.48%/1.82%), the participation of the MM and CF applications to system disruptions increased by ~5X and ~14X (71.44%/14.56% and 26.74%/1.96%) respectively.

5. CONCLUSIONS

It was presented a methodology aiming at enhancing SoC signal integrity to power-supply fluctuations. The goal is to keep circuit synchronism and nominal performance even in the presence of $V_{DD}$/$GND$ disturbances that, due to increased signal path delays, may cause IC de-synchronization. Typical solutions define, during design phase, conservative (reduced) IC clock rates to ensure synchronization between signal propagation through logic with clock control under power-supply grid disturbance.

The methodology is based on a clock duty cycle modulation (CDC Modulation) concept, which is built-up around a clock stretching logic (CSL) block. The CSL is used to monitor abnormal power interconnect activities ($V_{DD}$ undershoots or ground overshoots) and to enhance CDC proportionally to supply voltage variation. This solution is implemented by delaying the rising (or falling) edge of the clock signal, depending on which kind of D-FF is used in the controlled logic.

Practical experiments dealing with exposing a 32-bit soft-core pipeline processor to radiated electromagnetic interference (EMI) in a Gigahertz Transverse Electromagnetic (GTEM) Cell have been described. The Multiplier block of this processor was implemented and controlled according to the proposed technique. The whole processor was mapped into an FPGA device placed in a board designed and fabricated in partial compliance with the IEC standard 62.132 for radiated and conducted electromagnetic immunity measurements. The obtained results demonstrate that the measured processor robustness was increased in the order of 39.36% with respect to the same processor implemented without the CDC Modulation technique.

REFERENCES


