Session 4: Assertions and Transactions
2:00pm - 3:40pm
Assertion-based Verification of Behavioral Descriptions with Non-linear Solvers
J. Uiglitz, P. Sanchez, U. Cantabria
Efficient Automatic-Based Assertion Checker Synthesis of PLK Properties
N. Srivastava, C. Zanesco, M. Galletti, University of Michigan
Specification Language for Transaction Level Assertions
T. Horvath, V. Farkas, M. Holc, T. Steiner, M. Siller, Vienna
On the Automatic Transaction Generation for the TLM-based Design Flow
N. Bommuri, F. Fumio, U. Vesna
3:40pm - 4:00pm Break

Session 5: Test Case Generation II
4:00pm - 5:00pm
Addressing Test Generation Challenges for Configurable Processor Verification
J. Griswold, D. Jan, Texas A&M University
M. Minnis, J. Lang, J. Aili, J. Larsen, M. Vries, IBM Corp.
Deep Test - Extending the Model-based Approach to Functional Verification of Address Translation Mechanisms
K. Arai, Y. Kuzui, A. Igarashi, IBM
CP with Architectural State Lookup for Functional Test Generation
R. Goloborodko, A. Yee, Intel
Reusable On-Chip System Level Verification for Simulation Emulation and Silicon
A. Banerji, S. Ghandehari, H. Miller, D. Bell, R. Slater, O. Ban-Akaba, N. Lin, H. Bridge, Freescale

Keynote: J. Scott Runner, Qualcomm
6:00pm - 8:00pm Dinner Banquet
Title: Time to Quality: The Challenge of Verification Efficiency

FRIDAY, NOVEMBER 10
7:00 am - 8:00 am Continental Breakfast
7:00 am - 12:00 am Registration

Session 6: Transformation-based Verification
8:00am - 9:30am
Transaction Routing and its Verification by Correct Model Transformations
S. Aoki, D. Gupta, U. Calafiori, Intel
Taming the Complexity of STDV Design Verification Using Program Slicing
V. Ueda, T. Ando, A. Goiber, U. Texas, Austin

MDNB-Metadata-Based Microprocessor Verification Environment (short)
A. T. Dengkler, Intel
D. Markoukou, S. Sahu, Virginia Tech
S. Koulakis, D. Ily, U. Minnesota
9:00am - 9:25am Break

Session 7: Special Session II
9:25am - 10:40am
Dramatic Guided Hybrid Verification with GEIBO
V. Bartocci, U. Michigan
Everlast: A Flexible Platform for Industrial-Strength Abstract Guidance Simulation
A. Yu, U. British Columbia
Semi-Formal Verification at IBM
J. Ericstam, IBM Corp.
10:40am - 11:00am Break

Session 8: SAT and Equivalence Verification
11:00am - 12:30pm
Guiding CNF-SAT Search by Analyzing Constraint Variable Dependencies and Clause Lengths
V. Doring, P. Kael, U Utah
Equivalence Checking with Rule-Based Equivalence Propagation and High-Level Synthesis
T. Noliare, T. Koutavou, M. Fuji, U Tokyo
Practical Issues in Sequential Equivalence Checking through Allignability: Handling Don’t Care and Generating Delay Traces
L. More, B. Rave, C. Paille, Synopsys
IChecker: An Efficient Checker for Inductive Invariants (short)
F. Liu, T. Cheng, U California, Santa Barbara
12:30 - 2:00 Lunch

Session 9: Panel: Assertion-Based Verification - What is the Big Deal?
2:00pm - 3:30pm
Organizer: S. Sahu, Virginia Tech
Moderator: A. Hu, U. British Columbia
Panelists: TBD
3:30pm - 3:55pm Break

Session 10: System Level View and Modeling
3:55pm - 5:20pm
Runtime Deadlock Analysis of SystemsC Design
E. Chung, P. Tai, Y. Hsu, M. Hui, U California, Riverside
X. Chen, Nihao
Extracting a simplified view of design functionality via vector simulation
O. Guay, C. R. Hui, L. C. Wang, U California, Santa Barbara
T. Feng, Cadence, M. Freislof
A Tool for Automatic Detection of Deadlock in Wormhole Networks on Chip
S. Tatula, J. L. Orlandos, U Pisa 6
E. Enslen, ENI Calhoun & CNRS
Polychromatic Methodology for System Design: A True Concurrency Approach (short)
S. Sahu, D. Markoukou, S. Sahu, Virginia Tech
J. P. Talpin, India

Detailed information can be found on the HLDVT web site
http://www.hldvt.com/06/
Experience a hidden gem at Hyatt Regency Monterey. Play a round on Pebble Beach Company's championship Del Monte Golf Course, or perhaps a tennis lesson and game is more your style. Take a dip in the pools, followed by a pampering massage. Enjoy a wide array of dining choices in our luxury hotel in Monterey — including our famous sports bar. You'll delight in the deluxe amenities and unmatched service that await you at our Monterey, California hotel. For more information, visit the hotel website http://monterey.hyatt.com/

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Send full payment in U.S. dollars with this form. Use a check drawn on a US bank or a major credit card. For payments from non-US banks the attendee will be charged a collection fee of $20. Purchase orders are not accepted.
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Register before Tuesday, October 23, 2006, for the HLDVT’06 discounted room rate. Hotel space is limited. Please register before October 23, 2006, to avoid disappointment.

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