Delay Sensing for Parametric Variations and Defects Monitoring in Safety-Critical Applications

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Abstract — The impact of parametric variations on digital circuit performance is increasing in nanometer ICs, namely of PVT (Process, power supply Voltage and Temperature) variations. Moreover, circuit aging also impacts circuit performance, especially due to NBTI (Negative Bias Temperature Instability) effect. A growing number of physical defects manifest themselves as delay faults (at production, or during product lifetime). On-chip, on-line delay monitoring, as a circuit failure prediction technique, can be an attractive solution to guarantee correct operation in safety-critical applications. A novel delay sensor (to be selectively inserted in key locations in the design and to be activated according to user’s requirements) is proposed, and a 65 nm design is presented. The nanometer CMOS sensor is programmable, allowing delay monitoring for a wide range of delay values. The proposed sensor has been optimized to exhibit low sensitivity to PVT variations. Simulation results show that the sensor is effective on identifying abnormal delays, due to NBTI-induced aging and to resistive bridging defects.

Keywords: delay sensors, reliability in nanometer technologies, failure prediction, process variations, predictive delay fault detection.

I. INTRODUCTION

For safety-critical systems (e.g., automotive), digital system errors are unacceptable. Human lives are at stake. Reliable and dependable system operation is, thus, mandatory. In high-performance systems, the pace at which digital signal processing is carried out must be the fastest the physical system is able to deliver. Process variations and the majority of physical defects can be identified at production stage. Other parametric variations, namely VT (power supply Voltage and Temperature) variations, are operation-dependent. Nevertheless, they impact circuit performance. Many safety-critical applications products must operate for long periods of time (e.g., 10 years, for cars). Therefore, electronic aging [1], causing long-term performance degradation, must also be considered. In nanometer technologies, reliability problems increase [2][3], as well as variability. Long circuit operation may also activate latent physical defects. On-chip, on-line delay monitoring can be used to predict catastrophic time response and, thus, to prevent harm.

The purpose of this paper is to propose a methodology for delay monitoring of safety-critical digital systems, and to present a novel programmable delay sensor resilient to PVT (Process, power supply Voltage and Temperature) variations.

The paper is organized as follows. Section II briefly reviews PVT and aging phenomena, and their impact on system performance. Section III introduces the proposed delay monitoring methodology. In section IV, the delay sensor architecture is introduced. Section V briefly looks into the sensor’s physical design. In section VI, simulation results are presented. Finally, section VII summarizes the conclusions.

II. PVT AND AGING PHENOMENA

Parametric variations tend to increase with device scaling down. As a result, the safety margin associated with worst-case (WC) PVT variations becomes too wide, leading to unacceptable performance degradation. Moreover, electronic systems with long operation time exhibit long-term parametric variations, namely MOS threshold voltage (Vth) shifts, leading to performance degradation [3].

NBTI (Negative Bias Temperature Instability) is a dominant long-term effect in nanometer IC technologies [3]. It primarily affects PMOS transistors, when they are ON, enhancing |Vsa| along the time. Vsa degradation depends on time and on each PMOS device workload, which depends on circuit operation. However, Vsa degradation will ultimately cause a delay fault.

The impact of NBTI on digital circuit performance has been under research [4][3]. NBTI in static and dynamic operation has been modeled [5]. Recently, a circuit failure prediction technique has been proposed [6]. Agarwal et al. proposed an aging sensor [6] and presented its use on an experimental test chip [7]. Their major application was to reduce the pessimistic WC analysis associated with PVT variations.

Recently, an aging monitoring methodology, to be used during product lifetime, has been proposed [8], together with a new 0.35 μm CMOS sensor design, which exhibits a much lower sensitivity to VT variations than the Agrawal et al. sensor [6]. A new sensor topology, adequate for nanometer designs, has been proposed in [9].

III. DELAY MONITORING METHODOLOGY

For safety-critical applications, we propose to monitor the degrading timing response using on-line built-in delay
sensors. They are activated from time to time, to detect abnormal delays in critical paths, before they become catastrophic. If the timing degradation exceeds a given threshold, some preventive action is triggered, avoiding harm.

Being on-chip, the sensors must exhibit low sensitivity to operational conditions, namely to VT variations. In nanometer technologies, process variability is very large. Hence, the sensor must also exhibit low sensitivity to process (P) variations. Finally, in order to allow delay monitoring for a range of delay values, even in the presence of PVT variations, the sensor should be programmable.

The methodology comprises (1) development of new library cells, merging delay sensors with storage elements (FF); and (2) development of selective sensor insertion criteria. This paper focuses sensor design. Sensor insertion can be carried out at the output of each CUT (Circuit Under Test) critical path (CP). Due to PVT variations, we insert a sensor at the end of all the longest signal paths (e.g., τCP ∈ (0.9: 1.0) τCP). Long signal paths are identified with a STA (Static Timing Analysis) tool, like PrimeTime™. A more restrictive criterion can be used, to reduce overhead. For instance, if the primary cause of delay shifting is aging, an aging-aware STA procedure can be followed, as proposed in [7].

The proposed methodology is a circuit failure prediction technique and reuses several concepts presented in [6][7][8]. As the sensor detects abnormal delays, regardless of their origin, it can uncover (1) PVT variations and/or aging (namely, due to NBTI) and (2) delay faults due to physical defects activated by long circuit operation. Thus, sensor’s insertion enhances the internal observability of the timing degradation, before it is too late. We refer it as predictive delay detection.

IV. DELAY SENSOR

As shown in Fig. 1, delay sensors check critical path’s output signal (OUT_CL) transitions during a observation interval, Tg (referred as guardband interval in [6]).

The sensor has a delay element (DE, to define the observation interval, Tg); a stability checker (SC) and an output latch to store checker results. If, due to an abnormal propagation delay time, OUT_CL switches during the observation interval, OUT_AS=1.

Fig.1: CUT critical path, delay sensor, and capturing FF

The proposed delay sensor introduces a novel architecture, as compared to the sensors presented in [6] [8]. A new DE architecture is proposed. The new delay element retains the delay generation concept [8] using the charging/discharging time of a capacitor. However, a non-linear capacitor is used (MOSCAP-NP), composed of a NMOS and a PMOS transistor in parallel. This structure, referred as Complementary Gate Capacitor (CGC) in [10], exhibits low sensitivity to VDD variations.

Moreover, the current source / current mirror solution [8] is dropped, and substituted by a simple pull-up / pull-down (PD) programmable network, leading to significant area savings. The previous solution [8] exhibits low sensitivity to VT variations, due to current sources and mirrors use. The new DE has a slightly enhanced sensitivity to VT variations.

However, it does not compromise the sensor’s correct functionality in safety-critical applications.

![Delay Element Model](image1)

As shown in Fig. 2, NMOS transistors are used, as much as possible, to avoid the NBTI effect [4][5]. The NOR gate acts as an inverter only when PWD=0 (PWD is the signal to switch the sensor ON/OFF, Fig. 1). The remaining circuitry in Fig. 2 generates the OUT_GB signal. Signals OUT_GB and \( T_g \) determine the guardband interval width, \( T_g \), i.e., the period of time in which both signals are in the HIGH state.

Fig.2: Delay element of the proposed delay sensor

The MOSCAP-NP element, together with the input capacitance of the INV and the output capacitance of Mpab and the PD network, emulate a capacitor that, in the present 65 nm design, is \( C_v=15 \) fF. With MOSCAP-NP, at least one MOS transistor is in strong inversion region, showing much better capacitance linearity with VDD than a Simple Gate Capacitor. The proposed DE is a 15-MOSFET solution, much more compact than the Agrawal’s solution (23 MOSFET). Area savings, as compared to the aging sensor presented in [8], are even larger.

When the sensor is OFF (PWD=1), the output of the NOR gate is at logic ‘0’, Mpab will be ON, and \( V_{X}=V_{DD}, V_{OUT_GB}=0, \) and \( T_g=0 \). When the sensor is ON (PWD=0), the NOR gate generates \( \bar{T}_g=\bar{CLK} \). For \( DE=1 \), \( V_{X}=V_{DD} \) (pre-charge phase) and \( V_{OUT_GB}=0 \). However, for \( CLK=0, M_{NA1}, M_{SA2} \) and \( M_{NA3} \) will be ON and, depending on which additional transistors in the MOS network \( (M_{A1}, M_{A2} and M_{A3}) \) are activated too (driven by the HIGH logic value of A, B and C inputs), a pull-down network will be ON, discharging node X to ground and charging \( C_v \) capacitor to VDD. As \( V_X \) goes from \( V_{DD} \) to 0, \( V_{OUT_GB} \) switches 0→1, and a guardband interval is formed (\( T_g>0 \)).
With this architecture, \( T_g \) depends on the discharging time of node \( X \). The discharging current depends on the digital word \( DW = (A, B, C) \); hence, the sensor has a programmable \( T_g \), by selecting \( DW \). The lowest digital number (\( DW=001 \)) depicted in Fig. 4.

For the ST 65 nm technology, \( L_{\text{min}} = 60 \) nm. In our design, \( L_{\text{min}} = 65 \) nm. In [9], \( W_{\text{min}} = 100 \) nm. In the current design, \( W_{\text{min}} = 120 \) nm. The MOSCAP-NM is built with one NMOS and one PMOS transistors, both with \( W = L = 745 \) nm.

The stability checker and Latch configurations are shown in Fig. 3. When \( \text{CLK}=1 \), \( \text{OUT}_\text{SC}=0 \). During \( T_p, \text{CLKN} = \text{OUT}_\text{GB}=1 \), and \( \text{OUT}_\text{SC}=1 \) if and only if \( \text{OUT}_\text{CL} \) switches from 1\( \rightarrow \)0 or 0\( \rightarrow \)1.

The sensor physical design has been optimized with Astran for ST 65 nm technology. A version of the sensor layout is shown also in Fig. 5, where \( R_{\text{bridge}} \) is inserted (in XTRAN1) to emulate a typical resistive bridging defect between two internal nodes (X3 and G7).

![Fig.4: Aging sensor layout (ST 65 nm) (8.4 x 2.6 \( \mu \)m²)](image)

![Fig.5: CUT critical path considered in all simulations.](image)

The new sensor is analyzed under worst case (WC) VT conditions (\( V_{\text{DD}} = 72\% V_{\text{DDnom}} = 0.8 \) V, \( T = 180^\circ \)C). All circuit simulations are performed with HSPICE and PTM model [11].

Under WC conditions, the propagation delay time in the CUT’s critical path is \( t_{\text{PLH}} = 1.279 \) ns. The CLK period used in the simulations is \( T_{\text{CLK}} = 2.2 \) ns (50% duty cycle).

The dependence of \( t_{\text{PLH}} \) variation, \( \Delta t_{\text{PLH}} \), on \( V_{\text{DD}} \) variation, \( \Delta V_{\text{DD}} \) (NBTI aging), is shown in Fig. 6. Performance degradation is relevant, and significantly larger than the one observed in a similar CUT and a 0.35 \( \mu \)m IC technology [8].

In order to compare the sensitivity to VT variations of the proposed sensor and the one of Agrawal et al.’s [6], a replica of this sensor in 65 nm PTM was designed too. Fig. 7 shows \( T_g \) variations with \( V_{\text{DD}} \) and \( T \), for both sensors (for our sensor, \( DW = 7 \)). As shown, our sensor exhibits higher \( T_g \) values than Agrawal’s sensor, allowing the detection of lower propagation delay variations. For the same \( T_{\text{CLK}} \), Agrawal’s sensor can detect from 21.7 \% to 52\% in \( \Delta t_{\text{PLH}} \) (18\% to 34\% in \( \Delta V_{\text{DD}} \)). As expected, higher \( T \) or lower \( V_{\text{DD}} \) values decrease \( T_g \), due to the increase of the \( C_t \) discharging time.

Fig. 8 shows the levels of abnormal delay detection of the proposed sensor, for each digital word (DW). As shown, our sensor allows the detection of \( \Delta t_{\text{PLH}} \) due to aging from 17\% to 52\% (for a \( DW = 7 \)) and from 42\% to 52\% (with \( DW = 1 \)). The maximum value of \( \Delta t_{\text{PLH}} \) (52\%) depends on the time slack, which is determined by the clock frequency, \( f_{\text{CLK}} = 1/T_{\text{CLK}} \).
For safety-critical applications, the sensor must provide reliable operation also under P (Process) variations. Monte Carlo simulations have been performed, and are reported elsewhere [9]. Although the values of the range of \( \Delta t_{pd} \) depend on P variations, by varying DW, the sensor can be tuned to identify a specific \( \Delta t_{pd} \) variation.

The delay sensor can rewardingly be used for predictive delay testing. Bridging (BRI) defects are parametric defects, modeled by an \( R_{bridge} \) resistance. The value of \( R_{bridge} \) is unknown, and may drift, during product lifetime, according to workload conditions. From a user’s point of view, the \( R_{bridge} \) value is irrelevant. What is crucial is that, if the BRI defect manifests itself as an additional delay \( \Delta t_{pd} \), this abnormal delay should not exceed a given safety value, to prevent a circuit error. Hence, it is not important if the sensor can detect the bridging defect for the overall \( R_{bridge} \) range of values for which it is detectable. Instead, the goal is to make sure the proposed sensor is able to monitor the impact of the bridging defect within the range of \( R_{bridge} \) values for which it can become potentially harmful.

Injecting \( R_{bridge} \) in XTRAN1 (Fig. 5) disturbs \( t_{pd} \) of the critical path in the CUT. X3 is driven by an inverter. For VCUT VT conditions (\( V_{DD} = 0.8 \) V and \( T = 180^\circ C \)), Table 1 shows the detection range or \( R_{bridge} \) for different DW values.

For very high \( R_{bridge} \) values, the additional delay is so small that \( OUT\_CL \) does not fall into the observation interval, \( T_g \). For lower \( R_{bridge} \) values, the defect becomes detectable, as seen in Table 1. As expected, for high pull-down currents (high \( DW \), \( T_g \) is wider, and lower abnormal delays (due to \( R_{bridge} \)) are detectable (e.g., 25 kΩ for \( DW=7 \), 16.7 kΩ for \( DW=1 \)). Moreover, for \( R_{bridge} < 12.7 \) KΩ, the CUT’s output node does not respond (\( OUT\_CL=0 \), always stuck-at 0).

**Fig. 6:** \( \Delta \omega \) variations with \( \Delta V_{thP} \) aging variations for the CUT under study.

**Fig. 7:** \( T_g \) variations with \( T \) and \( V_{DD} \) for the two sensors ([6] and ours).

**Fig. 8:** Detection ranges in percent variations of \( t_{PLH} \) of the CUT under worst case conditions (\( V_{DD} = 0.8 \) V, \( T = 180^\circ C \)).

**Table 1:** Detection ranges for \( R_{bridge} \) for different digital words.

<table>
<thead>
<tr>
<th>Digital word</th>
<th>Detection Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>15.3 KΩ &lt; ( R_{bridge} ) &lt; 25 KΩ</td>
</tr>
<tr>
<td>6</td>
<td>15.3 KΩ &lt; ( R_{bridge} ) &lt; 23.6 KΩ</td>
</tr>
<tr>
<td>5</td>
<td>15.3 KΩ &lt; ( R_{bridge} ) &lt; 23.2 KΩ</td>
</tr>
<tr>
<td>4</td>
<td>15.3 KΩ &lt; ( R_{bridge} ) &lt; 21.3 KΩ</td>
</tr>
<tr>
<td>3</td>
<td>15.3 KΩ &lt; ( R_{bridge} ) &lt; 20.6 KΩ</td>
</tr>
<tr>
<td>2</td>
<td>15.3 KΩ &lt; ( R_{bridge} ) &lt; 17.7 KΩ</td>
</tr>
<tr>
<td>1</td>
<td>15.3 KΩ &lt; ( R_{bridge} ) &lt; 16.7 KΩ</td>
</tr>
</tbody>
</table>

VII. CONCLUSIONS

In this paper, a new methodology for delay monitoring of safety-critical digital systems, and a novel programmable delay sensor resilient to PVT variations have been presented.

Simulation results have shown that the sensor is effective in identifying abnormal delays, due to NBTI-induced aging, or to resistive BRI defects. Predictive delay testing is under research, and will be reported in the future.

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REFERENCES


